ZED Board	
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www.zedboard.org	
Function	**Sheet Number**
Cover Sheet	1
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FPGA Power	11
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DDR Termination	14
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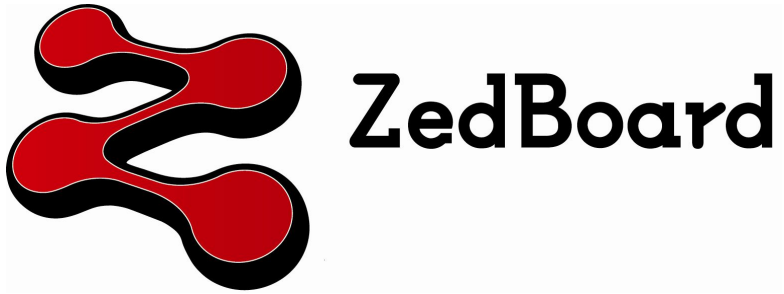

Revision F Changes
8 July 2020
- Re-routed PS-POR-B trace, which was causing cable plug events resulting in board reset, if the devices were at different ground potential.
- Re-named MODE nets so that their indices match Xilinx Zynq-7000 documentation
- Re-name VCFG nets to VMODE to match Xilinx Zynq-7000 documentation
- Added series termination resistors to buffered FMC JTAG lines.
- Reordered decoupling cap placement where not the lowest values were closest to the SoC
- Increase VCC1V0 nominal voltage by 19mV to allow for power distribution plane drop in high-current applications
- Changed L2, L4, L6 part numbers due to end-of-life.

Revision E Changes
16 Jan 2019
- Replaced micro USB receptacles with four-legged through-hole variant for greater mechanical stability
- Fixed IC1B floating OE# pin
- Interchanged VCC1V0 and VCC1V5 on power supply channels to allow for larger current on VCC1V0: <4A
- Ferrite bead FB13 was replaced by 0-ohm shunt.

Revision D Changes
29 Jan 2013
- Sheet 6: Replaced RJ-45 connector 1840808-7 (obsolete) with replacement 1840750-7
- Sheet 6: Added 50ohm series termination resistor to SD Clock signal
- Sheet 7: Modified C89 to 150uF to match USB requirements
- Sheet 7: Modified R150 connection to directly connect to pin 1 on J14
- Sheet 13: Modified DDR3 symbols to include missing pins
- Sheet 13: Modified CKE0 termination to connect to VTT rail
- Sheet 17: Added connectors to power heatsink fan

26 Feb 2013
- Sheet 4: Modified R87 to 10K to match datasheet recommendation
- Sheet 5: Modified R108 to show “No Load” status
- Sheet 16: Corrected typo

1 Mar 2013
- Sheet 1: Corrected typo
- Sheet 6: Removed R293 and note on termination placement, and added it to R293 circuit to sheet 10
- Sheet 13: Modified IC25, IC26 part number to MT41K128M16JT-125:K to match loaded part

Title	Rev
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Circuit	Title Page
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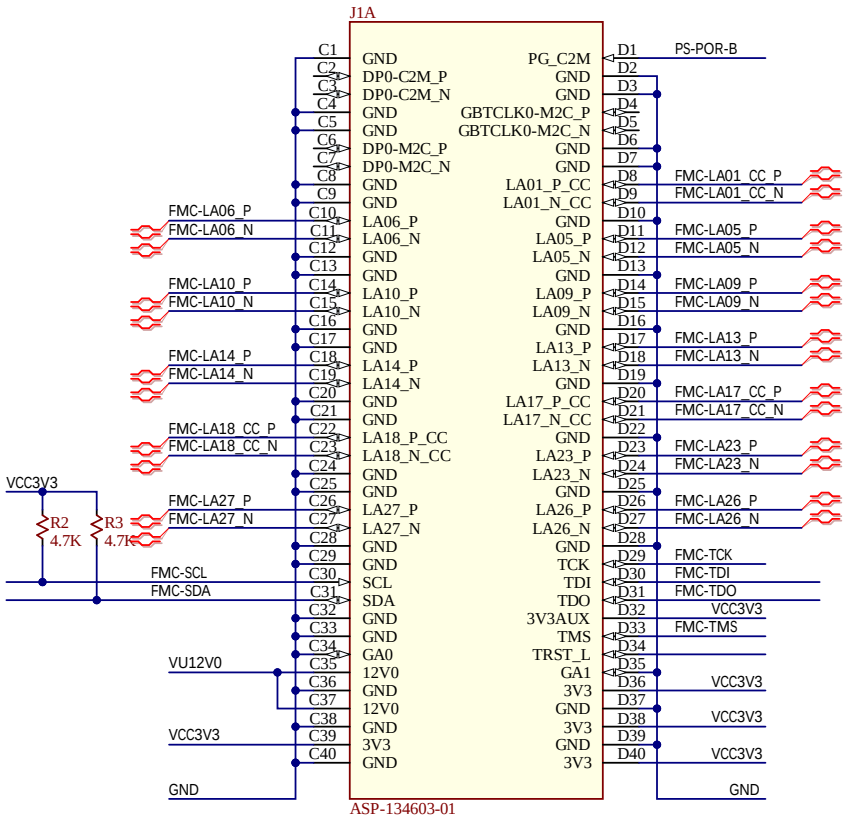

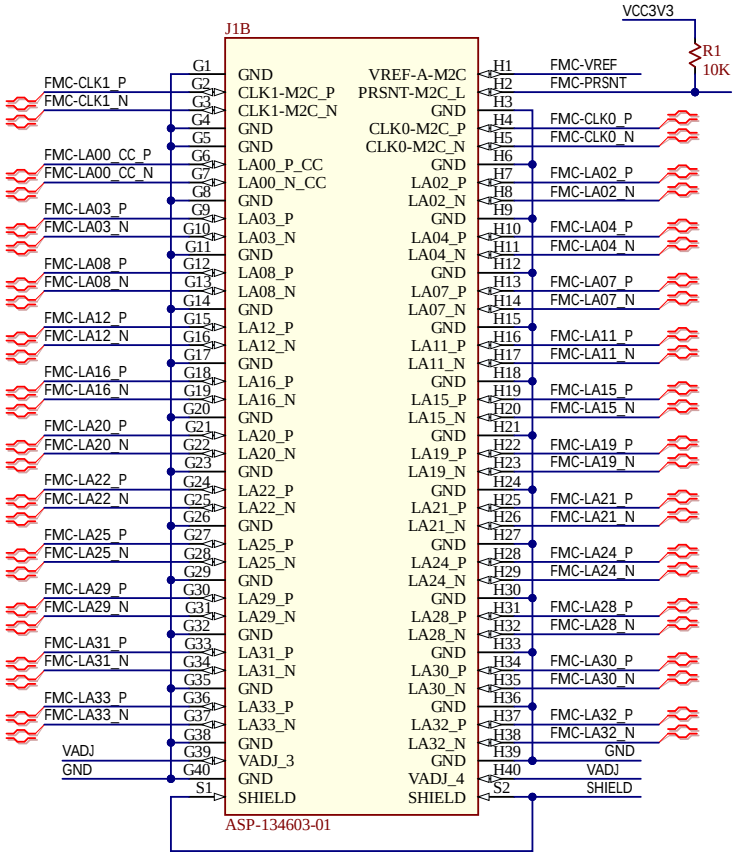

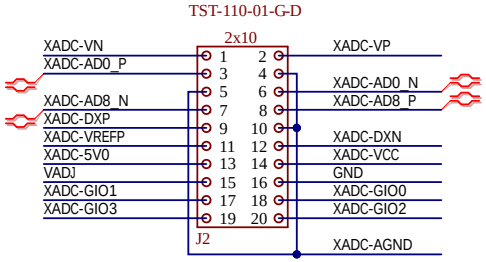

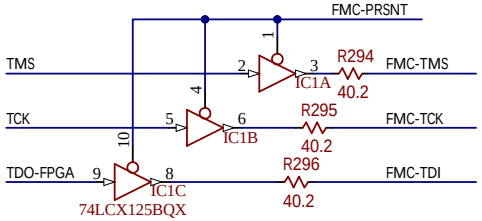

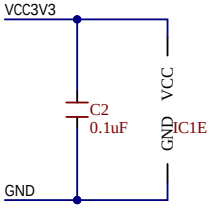

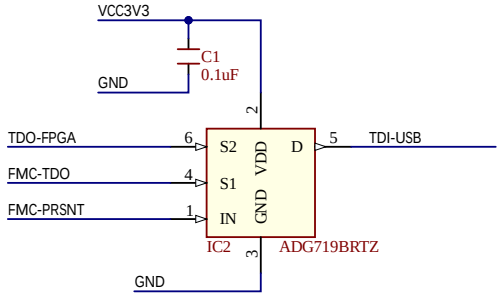

Foot F1
Foot F2
Foot F3
Foot F4

Title	Rev
ZED	F.1

Circuit	FMC and AMS Connector
Doc#	500-248
Engineer	EG
Author	GMA
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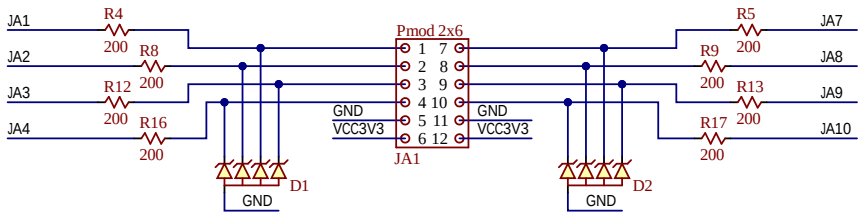
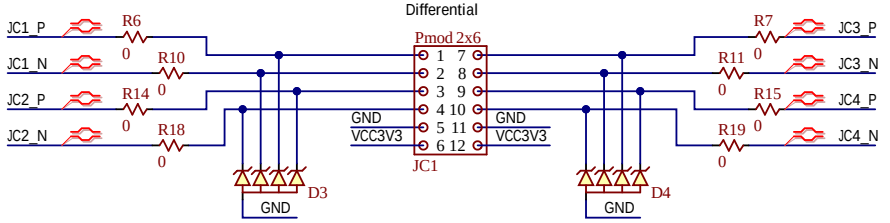
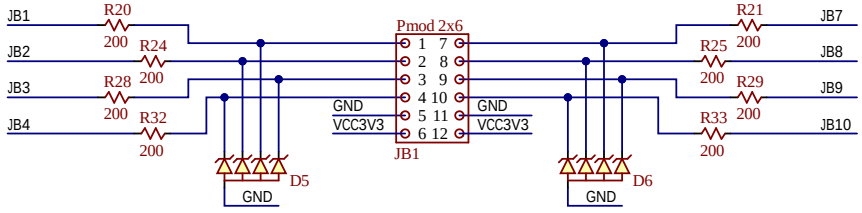
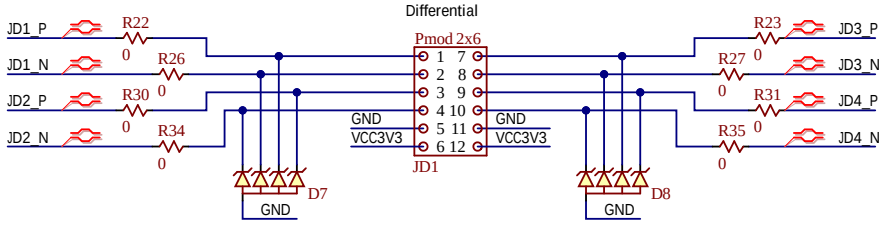
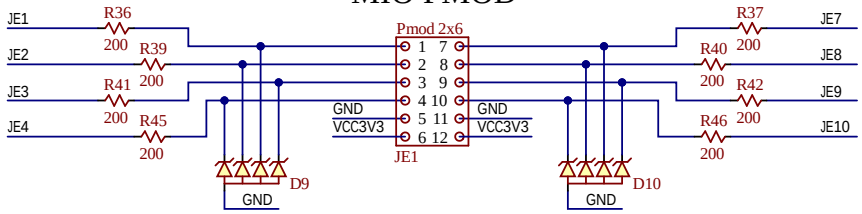




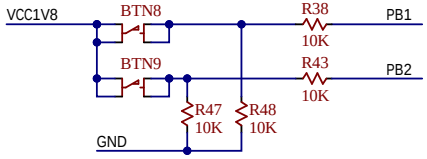


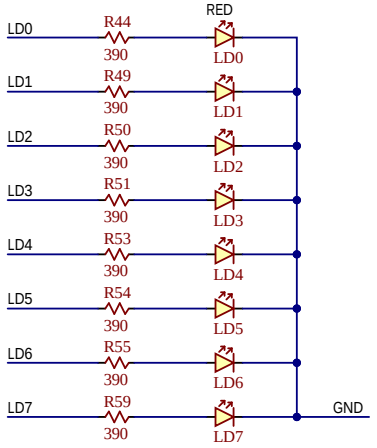


MIO PMOD

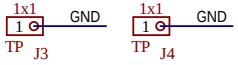


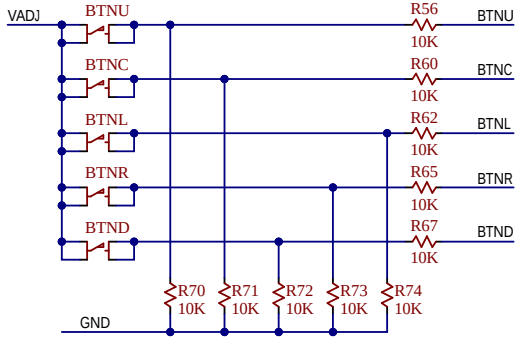
MIO BUTTON

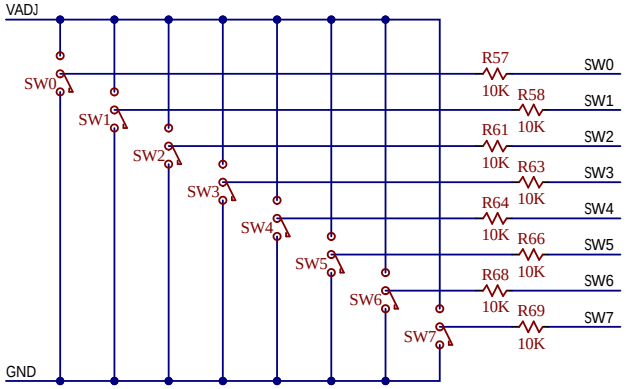




MIO LED







Title	ZED
Rev	F.1
Circuit	PMODs and General I/O
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Engineer	EG
Author	GMA
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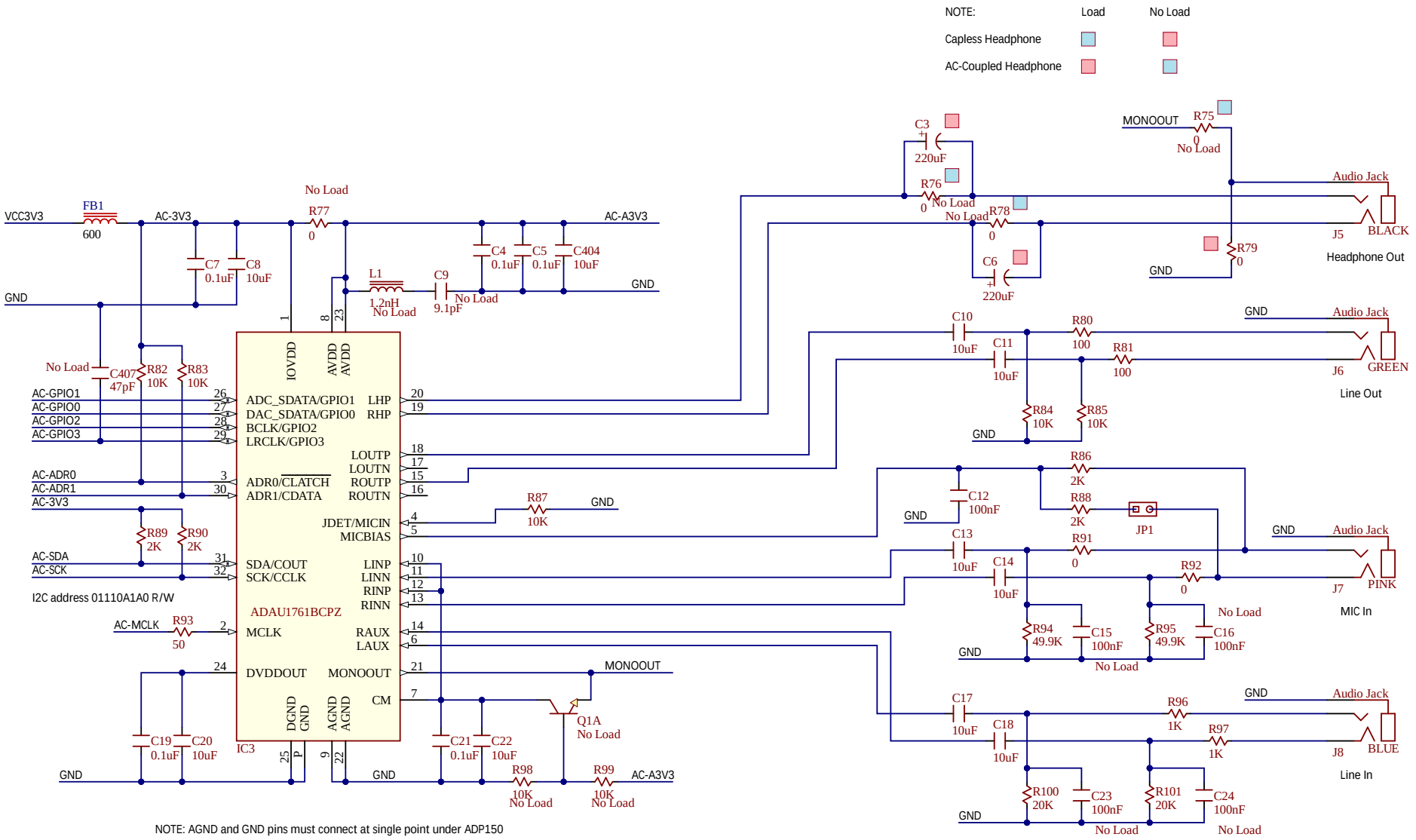
NOTE:
Load
No Load
Capless Headphone
AC-Coupled Headphone
VCC3V3
FB1
600
AC-3V3
No Load
R77
0
AC-A3V3
C7
0.1uF
C8
10uF
C4
0.1uF
C5
0.1uF
C404
10uF
GND
L1
1.2nH
No Load
C9
9.1pF
No Load
C3
220uF
R76
0
No Load
C6
220uF
No Load
R78
0
MONOOUT
R75
0
No Load
Audio Jack
J5
BLACK
Headphone Out
R79
0
GND
C10
10uF
C11
10uF
R80
100
R81
100
GND
Audio Jack
J6
GREEN
Line Out
R84
10K
R85
10K
GND
No Load
C407
47pF
R82
10K
R83
10K
AC-GPIO1
AC-GPIO0
AC-GPIO2
AC-GPIO3
AC-ADR0
AC-ADR1
AC-3V3
R89
2K
R90
2K
AC-SDA
AC-SCK
I2C address 01110A1A0 R/W
AC-MCLK
R93
50
IOVDD
AVDD
AVDD
ADC_SDATA/GPIO1
DAC_SDATA/GPIO0
BCLK/GPIO2
LRCLK/GPIO3
ADR0/CLATCH
ADR1/CDATA
SDA/COUT
SCK/CCLK
MCLK
DVDDOUT
DGND
GND
AGND
AGND
CM
LHP
RHP
LOUTP
LOUTN
ROUTP
ROUTN
JDET/MICIN
MICBIAS
LINP
LINN
RINP
RINN
RAUX
LAUX
MONOOUT
ADAU1761BCPZ
IC3
R87
10K
GND
C12
100nF
GND
R86
2K
R88
2K
JP1
C13
10uF
C14
10uF
R91
0
R92
0
GND
Audio Jack
J7
PINK
MIC In
R94
49.9K
C15
100nF
R95
49.9K
C16
100nF
No Load
No Load
GND
C17
10uF
C18
10uF
R96
1K
R97
1K
GND
Audio Jack
J8
BLUE
Line In
R100
20K
C23
100nF
R101
20K
C24
100nF
No Load
No Load
GND
C19
0.1uF
C20
10uF
GND
C21
0.1uF
C22
10uF
GND
Q1A
No Load
R98
10K
No Load
R99
10K
No Load
AC-A3V3
NOTE: AGND and GND pins must connect at single point under ADP150
VCC5V0
IC4
A1
B1
VIN
VOUT
EN
GND
A2
B2
ADP150ACBZ-3.3
C405
10uF
C25
1uF
GND
C26
1uF
C406
10uF
AC-A3V3
GND
Title
ZED
Rev
F.1
Circuit
Audio Codec
Doc# 500-248
Engineer EG
Author GMA
Date 10/20/2020
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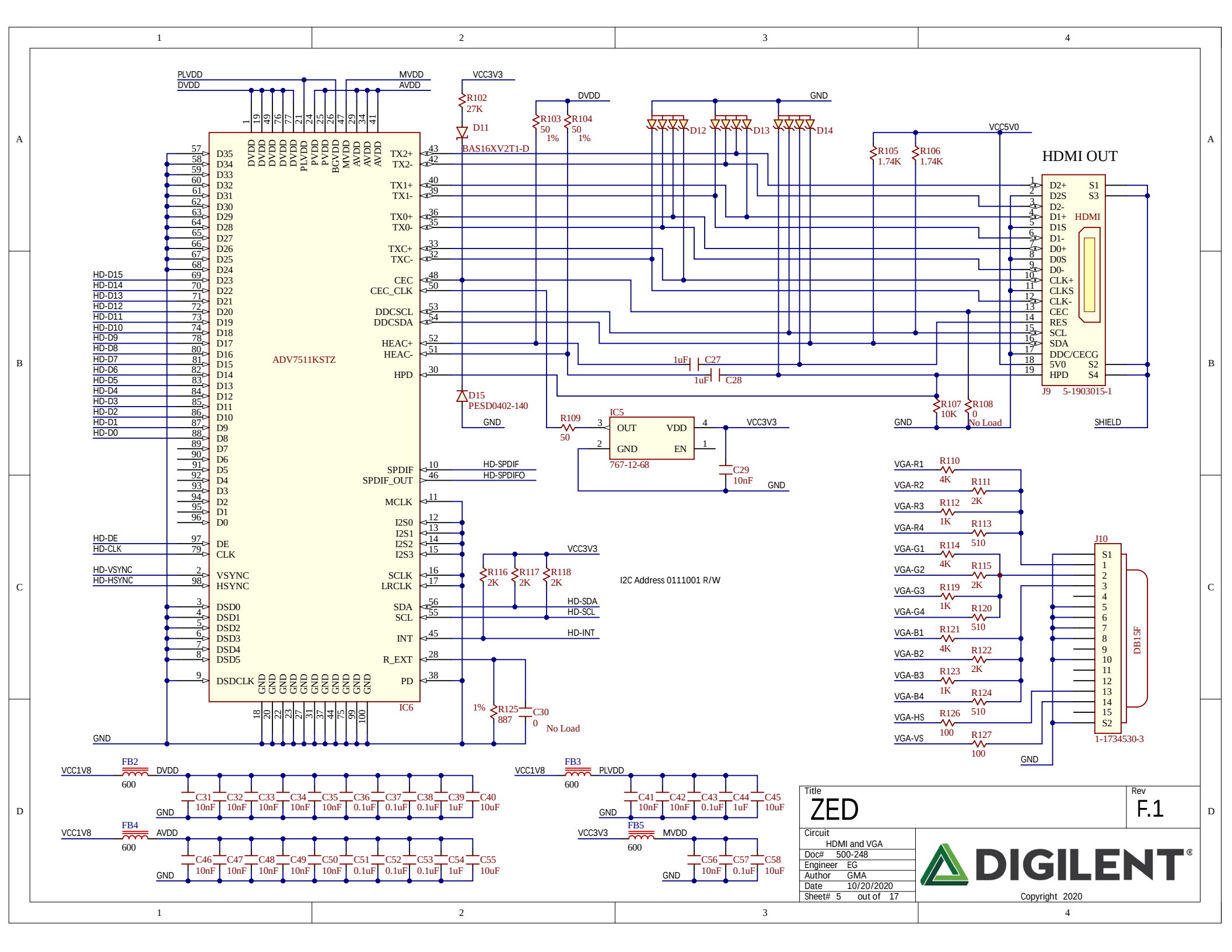
PLVDD
DVDD
MVDD
AVDD
VCC3V3
R102
27K
D11
BAS16XV2T1-D
DVDD
R103
50
1%
R104
50
1%
GND
D12
D13
D14
VCC5V0
R105
1.74K
R106
1.74K
HDMI OUT
ADV7511KSTZ
IC6
HD-D15
HD-D14
HD-D13
HD-D12
HD-D11
HD-D10
HD-D9
HD-D8
HD-D7
HD-D6
HD-D5
HD-D4
HD-D3
HD-D2
HD-D1
HD-D0
HD-DE
HD-CLK
HD-VSYNC
HD-HSYNC
TX2+
TX2-
TX1+
TX1-
TX0+
TX0-
TXC+
TXC-
CEC
CEC_CLK
DDCSCL
DDCSDA
HEAC+
HEAC-
HPD
SPDIF
SPDIF_OUT
MCLK
I2S0
I2S1
I2S2
I2S3
SCLK
LRCLK
SDA
SCL
INT
R_EXT
PD
HD-SPDIF
HD-SPDIFO
HD-SDA
HD-SCL
HD-INT
1uF
C27
1uF
C28
D15
PESD0402-140
R107
10K
R108
0
No Load
J9
5-1903015-1
HDMI
SHIELD
R109
50
IC5
OUT
VDD
GND
EN
767-12-68
C29
10nF
R116
2K
R117
2K
R118
2K
I2C Address 0111001 R/W
R125
887
C30
0
No Load
VGA-R1
VGA-R2
VGA-R3
VGA-R4
VGA-G1
VGA-G2
VGA-G3
VGA-G4
VGA-B1
VGA-B2
VGA-B3
VGA-B4
VGA-HS
VGA-VS
R110
4K
R111
2K
R112
1K
R113
510
R114
4K
R115
2K
R119
1K
R120
510
R121
4K
R122
2K
R123
1K
R124
510
R126
100
R127
100
J10
DB15F
1-1734530-3
FB2
600
FB3
600
FB4
600
FB5
600
VCC1V8
VCC3V3
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
C55
C56
C57
C58
10nF
0.1uF
1uF
Title
ZED
Rev
F.1
Circuit
HDMI and VGA
Doc# 500-248
Engineer EG
Author GMA
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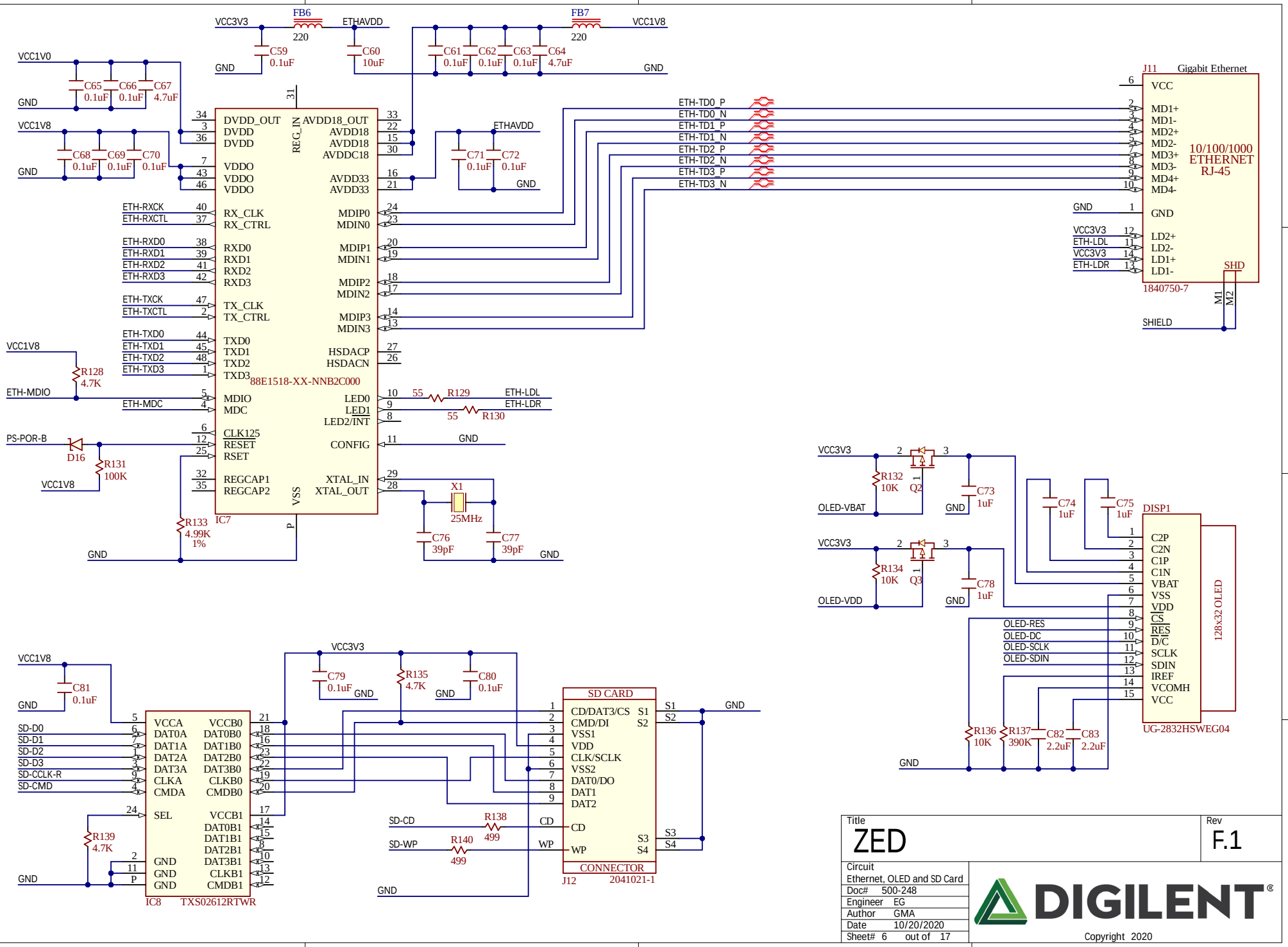
VCC3V3
FB6
220
ETHAVDD
C59
0.1uF
C60
10uF
GND
FB7
220
VCC1V8
C61
0.1uF
C62
0.1uF
C63
0.1uF
C64
4.7uF
VCC1V0
C65
0.1uF
C66
0.1uF
C67
4.7uF
C68
0.1uF
C69
0.1uF
C70
0.1uF
C71
0.1uF
C72
0.1uF
DVDD_OUT
DVDD
DVDD
REG_IN
AVDD18_OUT
AVDD18
AVDD18
AVDDC18
VDDO
VDDO
VDDO
AVDD33
AVDD33
RX_CLK
RX_CTRL
RXD0
RXD1
RXD2
RXD3
TX_CLK
TX_CTRL
TXD0
TXD1
TXD2
TXD3
MDIO
MDC
CLK125
RESET
RSET
REGCAP1
REGCAP2
VSS
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
HSDACP
HSDACN
LED0
LED1
LED2/INT
CONFIG
XTAL_IN
XTAL_OUT
P
88E1518-XX-NNB2C000
IC7
ETH-RXCK
ETH-RXCTL
ETH-RXD0
ETH-RXD1
ETH-RXD2
ETH-RXD3
ETH-TXCK
ETH-TXCTL
ETH-TXD0
ETH-TXD1
ETH-TXD2
ETH-TXD3
ETH-MDIO
ETH-MDC
ETH-TD0_P
ETH-TD0_N
ETH-TD1_P
ETH-TD1_N
ETH-TD2_P
ETH-TD2_N
ETH-TD3_P
ETH-TD3_N
R128
4.7K
R129
55
R130
55
ETH-LDL
ETH-LDR
PS-POR-B
D16
R131
100K
R133
4.99K
1%
X1
25MHz
C76
39pF
C77
39pF
J11
Gigabit Ethernet
VCC
MD1+
MD1-
MD2+
MD2-
MD3+
MD3-
MD4+
MD4-
GND
LD2+
LD2-
LD1+
LD1-
SHD
SHIELD
M1
M2
10/100/1000
ETHERNET
RJ-45
1840750-7
VCC3V3
ETH-LDL
ETH-LDR
R132
10K
Q2
R134
10K
Q3
OLED-VBAT
OLED-VDD
C73
1uF
C74
1uF
C75
1uF
C78
1uF
DISP1
C2P
C2N
C1P
C1N
VBAT
VSS
VDD
CS
RES
D/C
SCLK
SDIN
IREF
VCOMH
VCC
OLED-RES
OLED-DC
OLED-SCLK
OLED-SDIN
128x32 OLED
UG-2832HSWEG04
R136
10K
R137
390K
C82
2.2uF
C83
2.2uF
C81
0.1uF
C79
0.1uF
R135
4.7K
C80
0.1uF
VCCA
DAT0A
DAT1A
DAT2A
DAT3A
CLKA
CMDA
SEL
VCCB0
DAT0B0
DAT1B0
DAT2B0
DAT3B0
CLKB0
CMDB0
VCCB1
DAT0B1
DAT1B1
DAT2B1
DAT3B1
CLKB1
CMDB1
TXS02612RTWR
IC8
SD-D0
SD-D1
SD-D2
SD-D3
SD-CCLK-R
SD-CMD
R139
4.7K
SD CARD
CD/DAT3/CS
CMD/DI
VSS1
VDD
CLK/SCLK
VSS2
DAT0/DO
DAT1
DAT2
CD
WP
S1
S2
S3
S4
CONNECTOR
J12
2041021-1
SD-CD
SD-WP
R138
499
R140
499
Title
ZED
Rev
F.1
Circuit
Ethernet, OLED and SD Card
Doc# 500-248
Engineer EG
Author GMA
Date 10/20/2020
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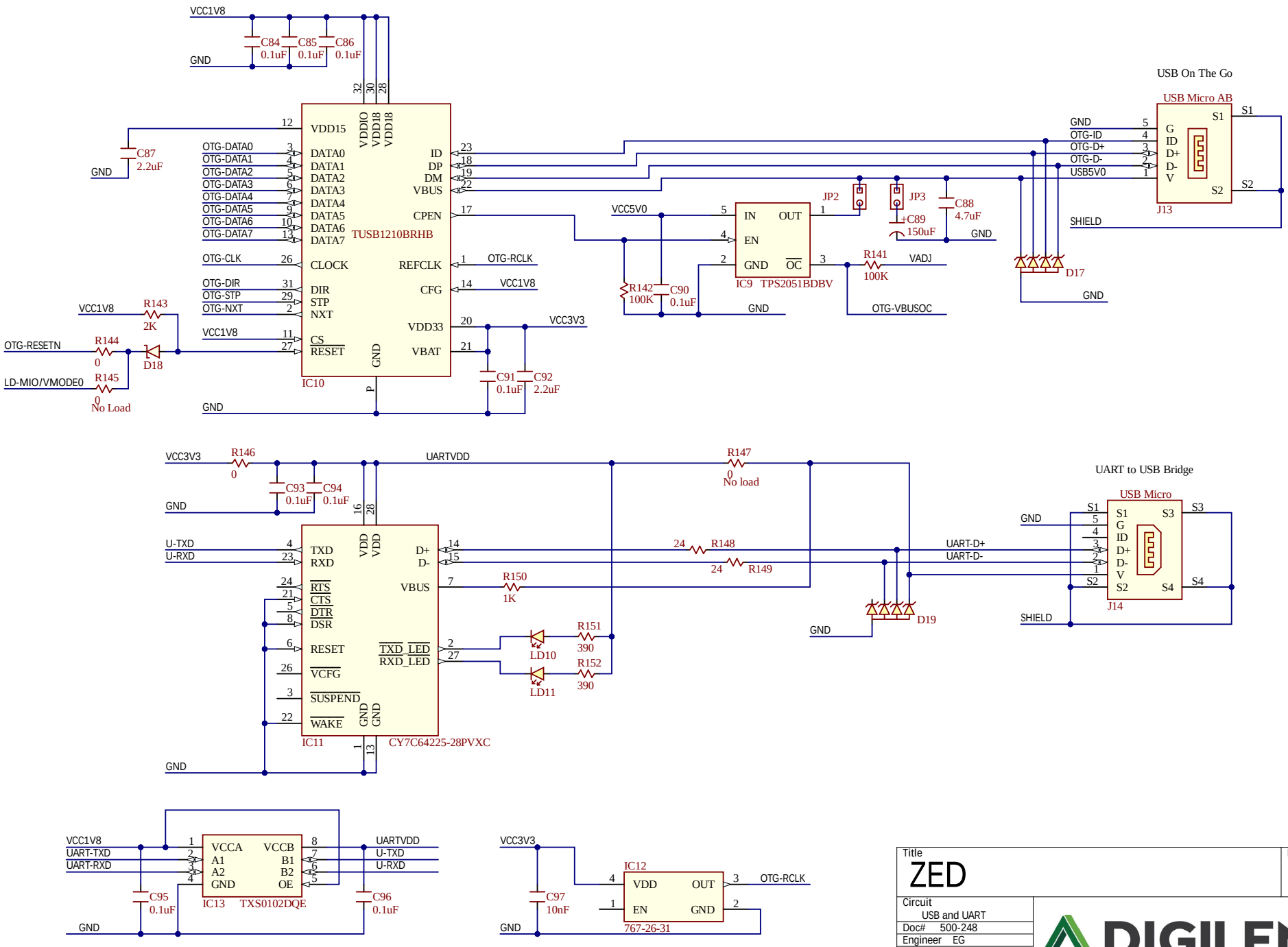

Title	ZED
Rev	F.1
Circuit	USB and UART
Doc#	500-248
Engineer	EG
Author	GMA
Date	10/20/2020
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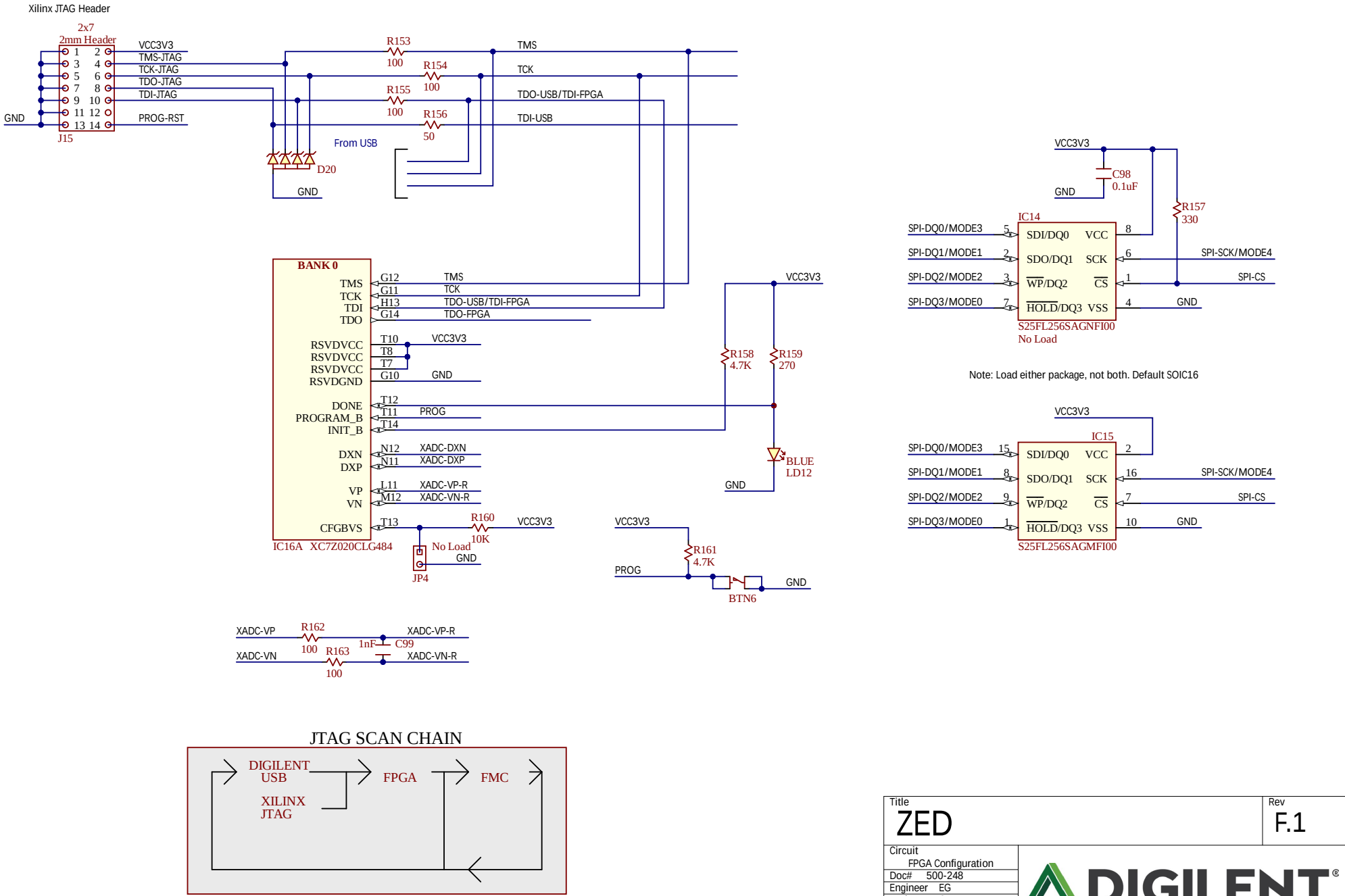

Title	ZED
Rev	F.1
Circuit	FPGA Configuration
Doc#	500-248
Engineer	EG
Author	GMA
Date	10/20/2020
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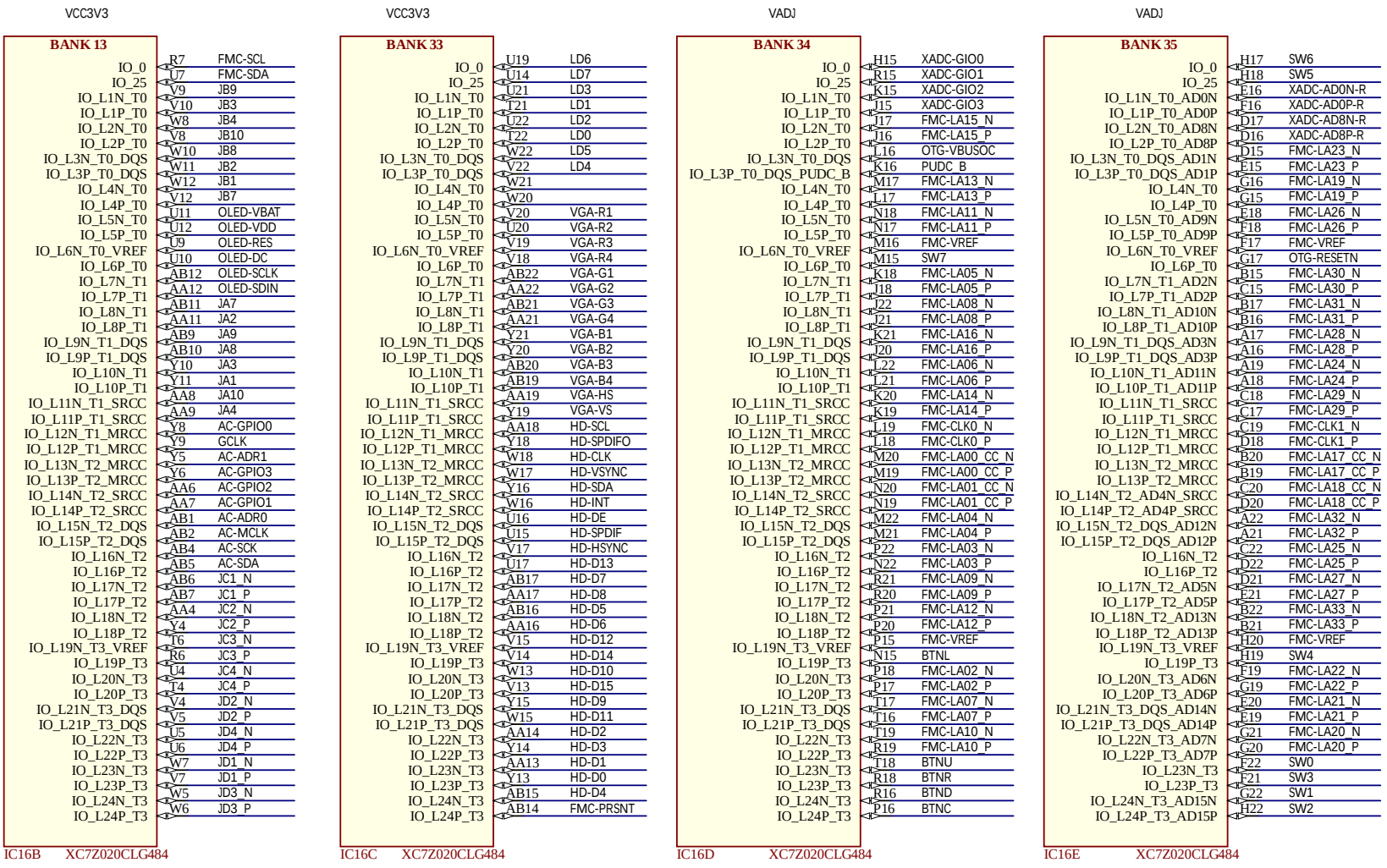
VCC3V3
BANK 13
IO_0 R7 FMC-SCL
IO_25 U7 FMC-SDA
IO_L1N_T0 V9 JB9
IO_L1P_T0 V10 JB3
IO_L2N_T0 W8 JB4
IO_L2P_T0 V8 JB10
IO_L3N_T0_DQS W10 JB8
IO_L3P_T0_DQS W11 JB2
IO_L4N_T0 W12 JB1
IO_L4P_T0 V12 JB7
IO_L5N_T0 U11 OLED-VBAT
IO_L5P_T0 U12 OLED-VDD
IO_L6N_T0_VREF U9 OLED-RES
IO_L6P_T0 U10 OLED-DC
IO_L7N_T1 AB12 OLED-SCLK
IO_L7P_T1 AA12 OLED-SDIN
IO_L8N_T1 AB11 JA7
IO_L8P_T1 AA11 JA2
IO_L9N_T1_DQS AB9 JA9
IO_L9P_T1_DQS AB10 JA8
IO_L10N_T1 Y10 JA3
IO_L10P_T1 Y11 JA1
IO_L11N_T1_SRCC AA8 JA10
IO_L11P_T1_SRCC AA9 JA4
IO_L12N_T1_MRCC Y8 AC-GPIO0
IO_L12P_T1_MRCC Y9 GCLK
IO_L13N_T2_MRCC Y5 AC-ADR1
IO_L13P_T2_MRCC Y6 AC-GPIO3
IO_L14N_T2_SRCC AA6 AC-GPIO2
IO_L14P_T2_SRCC AA7 AC-GPIO1
IO_L15N_T2_DQS AB1 AC-ADR0
IO_L15P_T2_DQS AB2 AC-MCLK
IO_L16N_T2 AB4 AC-SCK
IO_L16P_T2 AB5 AC-SDA
IO_L17N_T2 AB6 JC1_N
IO_L17P_T2 AB7 JC1_P
IO_L18N_T2 AA4 JC2_N
IO_L18P_T2 Y4 JC2_P
IO_L19N_T3_VREF T6 JC3_N
IO_L19P_T3 R6 JC3_P
IO_L20N_T3 U4 JC4_N
IO_L20P_T3 T4 JC4_P
IO_L21N_T3_DQS V4 JD2_N
IO_L21P_T3_DQS V5 JD2_P
IO_L22N_T3 U5 JD4_N
IO_L22P_T3 U6 JD4_P
IO_L23N_T3 W7 JD1_N
IO_L23P_T3 V7 JD1_P
IO_L24N_T3 W5 JD3_N
IO_L24P_T3 W6 JD3_P
IC16B XC7Z020CLG484
VCC3V3
BANK 33
IO_0 U19 LD6
IO_25 U14 LD7
IO_L1N_T0 U21 LD3
IO_L1P_T0 T21 LD1
IO_L2N_T0 U22 LD2
IO_L2P_T0 T22 LD0
IO_L3N_T0_DQS W22 LD5
IO_L3P_T0_DQS V22 LD4
IO_L4N_T0 W21
IO_L4P_T0 W20
IO_L5N_T0 V20 VGA-R1
IO_L5P_T0 U20 VGA-R2
IO_L6N_T0_VREF V19 VGA-R3
IO_L6P_T0 V18 VGA-R4
IO_L7N_T1 AB22 VGA-G1
IO_L7P_T1 AA22 VGA-G2
IO_L8N_T1 AB21 VGA-G3
IO_L8P_T1 AA21 VGA-G4
IO_L9N_T1_DQS Y21 VGA-B1
IO_L9P_T1_DQS Y20 VGA-B2
IO_L10N_T1 AB20 VGA-B3
IO_L10P_T1 AB19 VGA-B4
IO_L11N_T1_SRCC AA19 VGA-HS
IO_L11P_T1_SRCC Y19 VGA-VS
IO_L12N_T1_MRCC AA18 HD-SCL
IO_L12P_T1_MRCC Y18 HD-SPDIFO
IO_L13N_T2_MRCC W18 HD-CLK
IO_L13P_T2_MRCC W17 HD-VSYNC
IO_L14N_T2_SRCC Y16 HD-SDA
IO_L14P_T2_SRCC W16 HD-INT
IO_L15N_T2_DQS U16 HD-DE
IO_L15P_T2_DQS U15 HD-SPDIF
IO_L16N_T2 V17 HD-HSYNC
IO_L16P_T2 U17 HD-D13
IO_L17N_T2 AB17 HD-D7
IO_L17P_T2 AA17 HD-D8
IO_L18N_T2 AB16 HD-D5
IO_L18P_T2 AA16 HD-D6
IO_L19N_T3_VREF V15 HD-D12
IO_L19P_T3 V14 HD-D14
IO_L20N_T3 W13 HD-D10
IO_L20P_T3 V13 HD-D15
IO_L21N_T3_DQS Y15 HD-D9
IO_L21P_T3_DQS W15 HD-D11
IO_L22N_T3 AA14 HD-D2
IO_L22P_T3 Y14 HD-D3
IO_L23N_T3 AA13 HD-D1
IO_L23P_T3 Y13 HD-D0
IO_L24N_T3 AB15 HD-D4
IO_L24P_T3 AB14 FMC-PRSNT
IC16C XC7Z020CLG484
VADJ
BANK 34
IO_0 H15 XADC-GIO0
IO_25 R15 XADC-GIO1
IO_L1N_T0 K15 XADC-GIO2
IO_L1P_T0 J15 XADC-GIO3
IO_L2N_T0 J17 FMC-LA15_N
IO_L2P_T0 J16 FMC-LA15_P
IO_L3N_T0_DQS L16 OTG-VBUSOC
IO_L3P_T0_DQS_PUDC_B K16 PUDC_B
IO_L4N_T0 M17 FMC-LA13_N
IO_L4P_T0 L17 FMC-LA13_P
IO_L5N_T0 N18 FMC-LA11_N
IO_L5P_T0 N17 FMC-LA11_P
IO_L6N_T0_VREF M16 FMC-VREF
IO_L6P_T0 M15 SW7
IO_L7N_T1 K18 FMC-LA05_N
IO_L7P_T1 J18 FMC-LA05_P
IO_L8N_T1 J22 FMC-LA08_N
IO_L8P_T1 J21 FMC-LA08_P
IO_L9N_T1_DQS K21 FMC-LA16_N
IO_L9P_T1_DQS J20 FMC-LA16_P
IO_L10N_T1 L22 FMC-LA06_N
IO_L10P_T1 L21 FMC-LA06_P
IO_L11N_T1_SRCC K20 FMC-LA14_N
IO_L11P_T1_SRCC K19 FMC-LA14_P
IO_L12N_T1_MRCC L19 FMC-CLK0_N
IO_L12P_T1_MRCC L18 FMC-CLK0_P
IO_L13N_T2_MRCC M20 FMC-LA00_CC_N
IO_L13P_T2_MRCC M19 FMC-LA00_CC_P
IO_L14N_T2_SRCC N20 FMC-LA01_CC_N
IO_L14P_T2_SRCC N19 FMC-LA01_CC_P
IO_L15N_T2_DQS M22 FMC-LA04_N
IO_L15P_T2_DQS M21 FMC-LA04_P
IO_L16N_T2 P22 FMC-LA03_N
IO_L16P_T2 N22 FMC-LA03_P
IO_L17N_T2 R21 FMC-LA09_N
IO_L17P_T2 R20 FMC-LA09_P
IO_L18N_T2 P21 FMC-LA12_N
IO_L18P_T2 P20 FMC-LA12_P
IO_L19N_T3_VREF P15 FMC-VREF
IO_L19P_T3 N15 BTNL
IO_L20N_T3 P18 FMC-LA02_N
IO_L20P_T3 P17 FMC-LA02_P
IO_L21N_T3_DQS T17 FMC-LA07_N
IO_L21P_T3_DQS T16 FMC-LA07_P
IO_L22N_T3 T19 FMC-LA10_N
IO_L22P_T3 R19 FMC-LA10_P
IO_L23N_T3 T18 BTNU
IO_L23P_T3 R18 BTNR
IO_L24N_T3 R16 BTND
IO_L24P_T3 P16 BTNC
IC16D XC7Z020CLG484
VADJ
BANK 35
IO_0 H17 SW6
IO_25 H18 SW5
IO_L1N_T0_AD0N E16 XADC-AD0N-R
IO_L1P_T0_AD0P E16 XADC-AD0P-R
IO_L2N_T0_AD8N D17 XADC-AD8N-R
IO_L2P_T0_AD8P D16 XADC-AD8P-R
IO_L3N_T0_DQS_AD1N D15 FMC-LA23_N
IO_L3P_T0_DQS_AD1P E15 FMC-LA23_P
IO_L4N_T0 G16 FMC-LA19_N
IO_L4P_T0 G15 FMC-LA19_P
IO_L5N_T0_AD9N E18 FMC-LA26_N
IO_L5P_T0_AD9P F18 FMC-LA26_P
IO_L6N_T0_VREF F17 FMC-VREF
IO_L6P_T0 G17 OTG-RESETN
IO_L7N_T1_AD2N B15 FMC-LA30_N
IO_L7P_T1_AD2P C15 FMC-LA30_P
IO_L8N_T1_AD10N B17 FMC-LA31_N
IO_L8P_T1_AD10P B16 FMC-LA31_P
IO_L9N_T1_DQS_AD3N A17 FMC-LA28_N
IO_L9P_T1_DQS_AD3P A16 FMC-LA28_P
IO_L10N_T1_AD11N A19 FMC-LA24_N
IO_L10P_T1_AD11P A18 FMC-LA24_P
IO_L11N_T1_SRCC C18 FMC-LA29_N
IO_L11P_T1_SRCC C17 FMC-LA29_P
IO_L12N_T1_MRCC G19 FMC-CLK1_N
IO_L12P_T1_MRCC D18 FMC-CLK1_P
IO_L13N_T2_MRCC B20 FMC-LA17_CC_N
IO_L13P_T2_MRCC B19 FMC-LA17_CC_P
IO_L14N_T2_AD4N_SRCC C20 FMC-LA18_CC_N
IO_L14P_T2_AD4P_SRCC D20 FMC-LA18_CC_P
IO_L15N_T2_DQS_AD12N A22 FMC-LA32_N
IO_L15P_T2_DQS_AD12P A21 FMC-LA32_P
IO_L16N_T2 C22 FMC-LA25_N
IO_L16P_T2 D22 FMC-LA25_P
IO_L17N_T2_AD5N D21 FMC-LA27_N
IO_L17P_T2_AD5P E21 FMC-LA27_P
IO_L18N_T2_AD13N B22 FMC-LA33_N
IO_L18P_T2_AD13P B21 FMC-LA33_P
IO_L19N_T3_VREF H20 FMC-VREF
IO_L19P_T3 H19 SW4
IO_L20N_T3_AD6N F19 FMC-LA22_N
IO_L20P_T3_AD6P G19 FMC-LA22_P
IO_L21N_T3_DQS_AD14N E20 FMC-LA21_N
IO_L21P_T3_DQS_AD14P E19 FMC-LA21_P
IO_L22N_T3_AD7N G21 FMC-LA20_N
IO_L22P_T3_AD7P G20 FMC-LA20_P
IO_L23N_T3 F22 SW0
IO_L23P_T3 F21 SW3
IO_L24N_T3_AD15N G22 SW1
IO_L24P_T3_AD15P H22 SW2
IC16E XC7Z020CLG484
PUDC_B R164 1K R165 10K VADJ
No Load JP5 GND
VCC3V3
IC17
VDD OUT GCLK
EN GND
C101 10nF
GND
767-100-136
XADC-AD0_N R166 100 1nF C100 XADC-AD0N-R
XADC-AD0_P R167 100 XADC-AD0P-R
XADC-AD8_N R168 100 1nF C102 XADC-AD8N-R
XADC-AD8_P R169 100 XADC-AD8P-R
Title
ZED
Rev
F.1
Circuit
FPGA Banks
Doc# 500-248
Engineer EG
Author GMA
Date 10/20/2020
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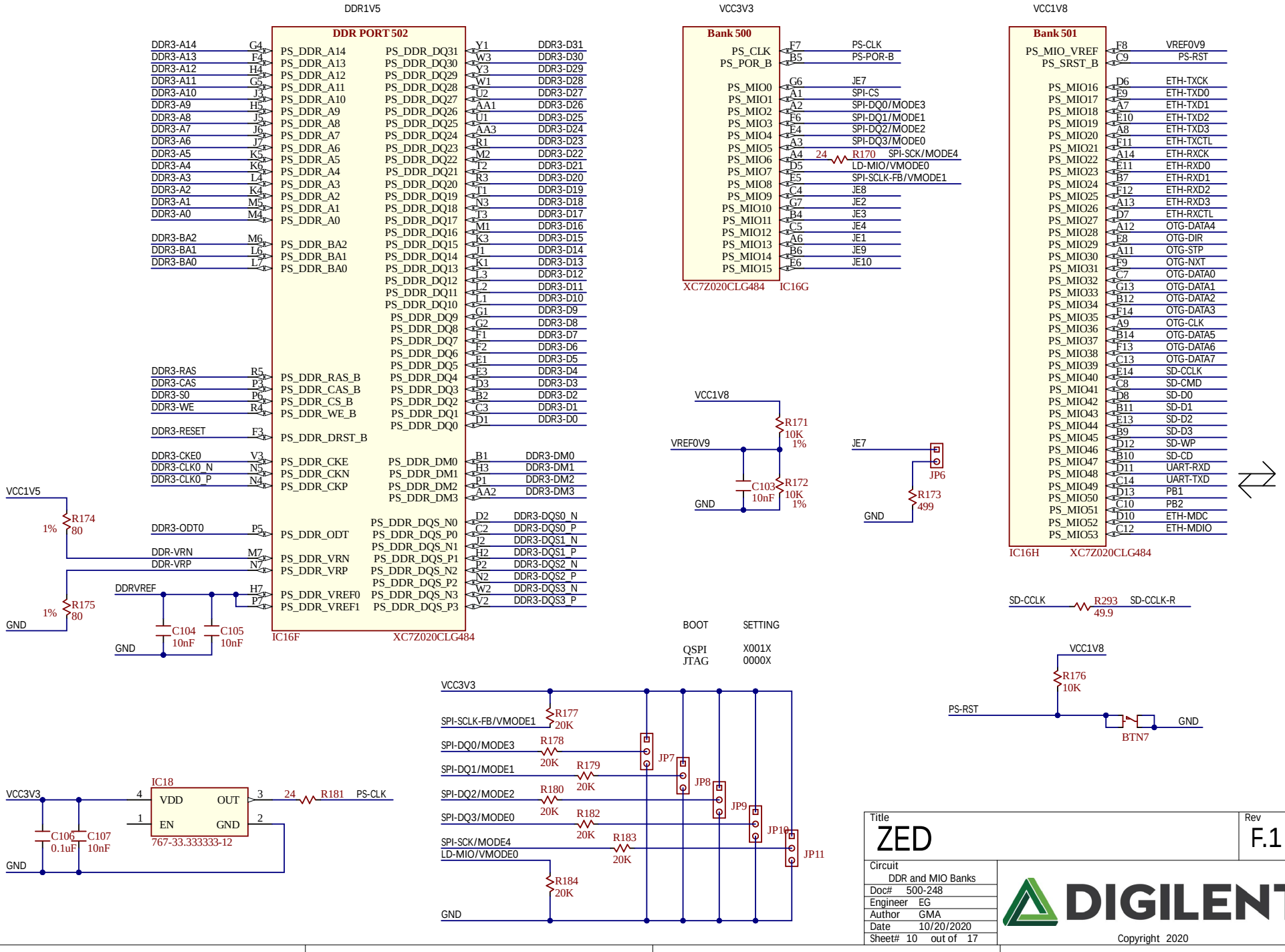
DDR1V5
DDR PORT 502
IC16F
XC7Z020CLG484
VCC3V3
Bank 500
XC7Z020CLG484
IC16G
VCC1V8
Bank 501
IC16H
XC7Z020CLG484
BOOT SETTING
QSPI X001X
JTAG 0000X
Title
ZED
Rev
F.1
Circuit
DDR and MIO Banks
Doc# 500-248
Engineer EG
Author GMA
Date 10/20/2020
Sheet# 10 out of 17
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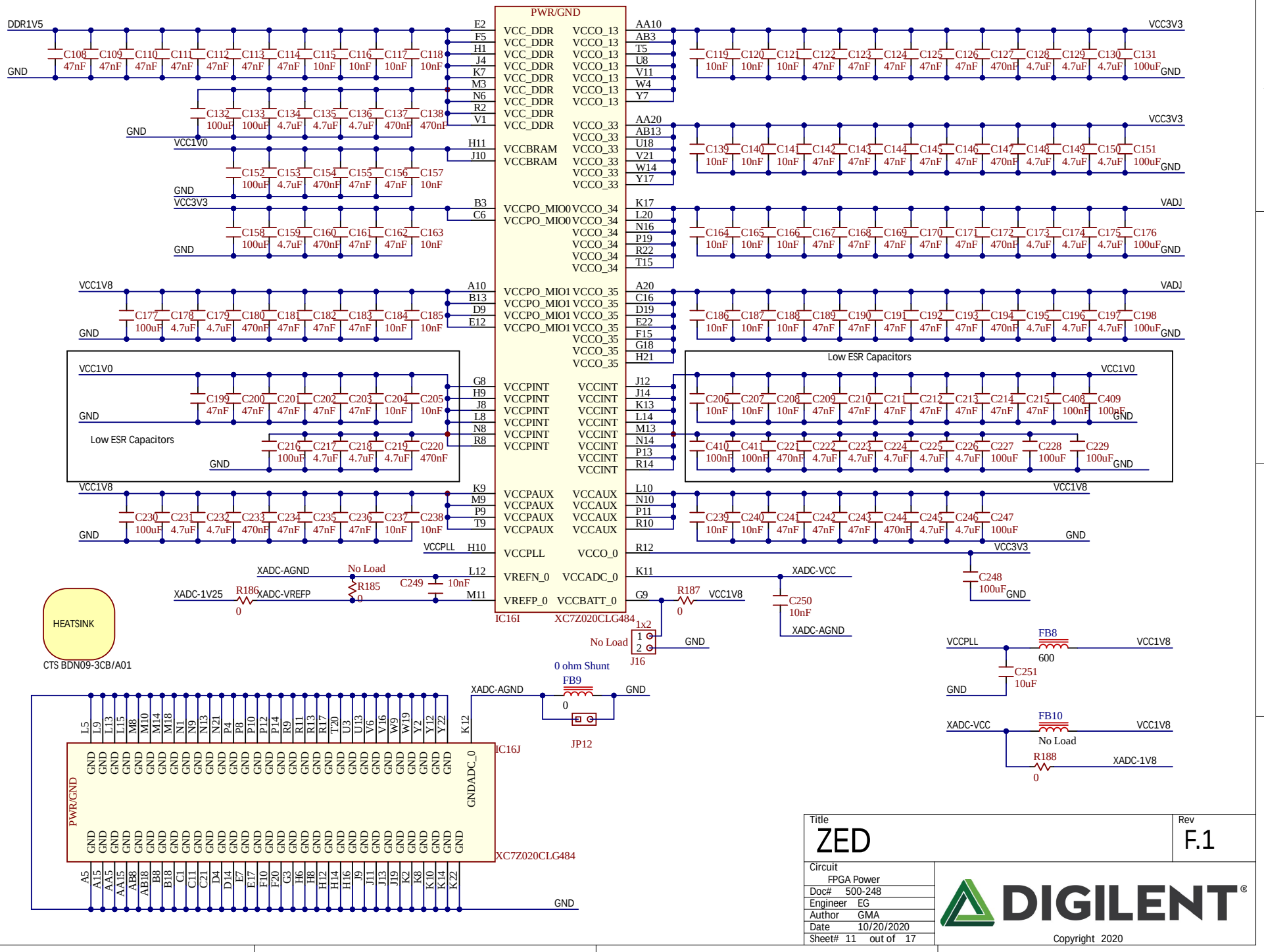

Title	ZED
Rev	F.1
Circuit	FPGA Power
Doc#	500-248
Engineer	EG
Author	GMA
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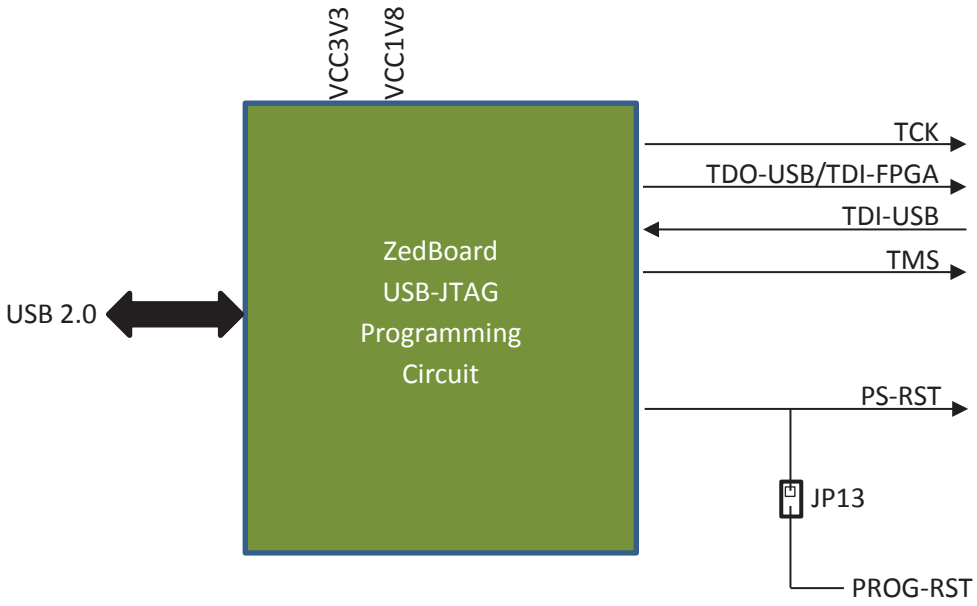

The ZedBoard contains a proprietary USB-JTAG circuit which is obscured on this sheet. This circuit contains IC19, IC20, IC21, IC22, IC23, IC24, JP13, and J17, along with a number of resistors and capacitors. The firmware for this circuit is not publicly available. However, the firmware does come pre-programmed in the SMT2 USB-JTAG module available from Digilent and Avnet.

Title	Rev
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Circuit	USB Programming
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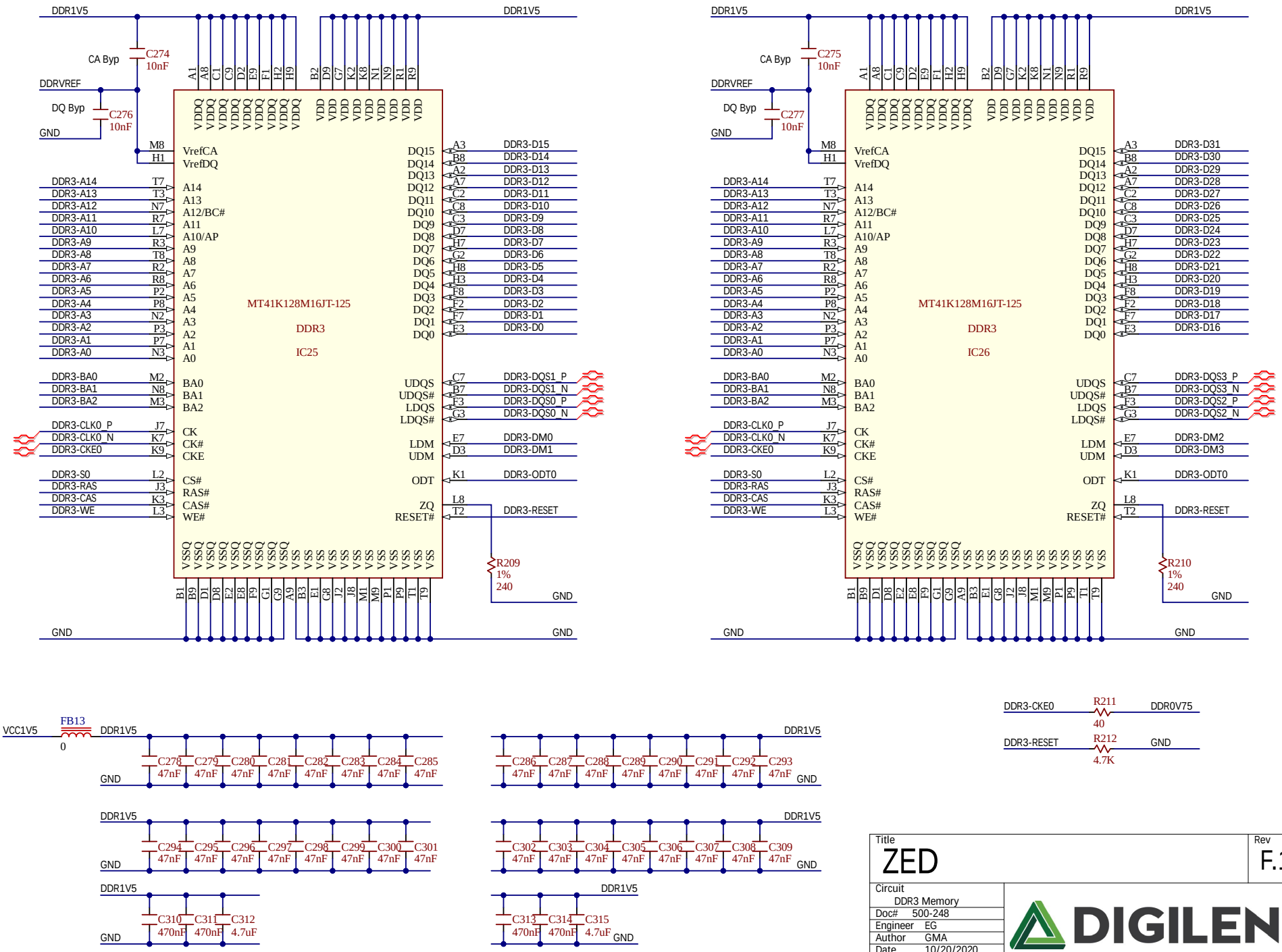

Title	ZED
Rev	F.1
Circuit	DDR3 Memory
Doc#	500-248
Engineer	EG
Author	GMA
Date	10/20/2020
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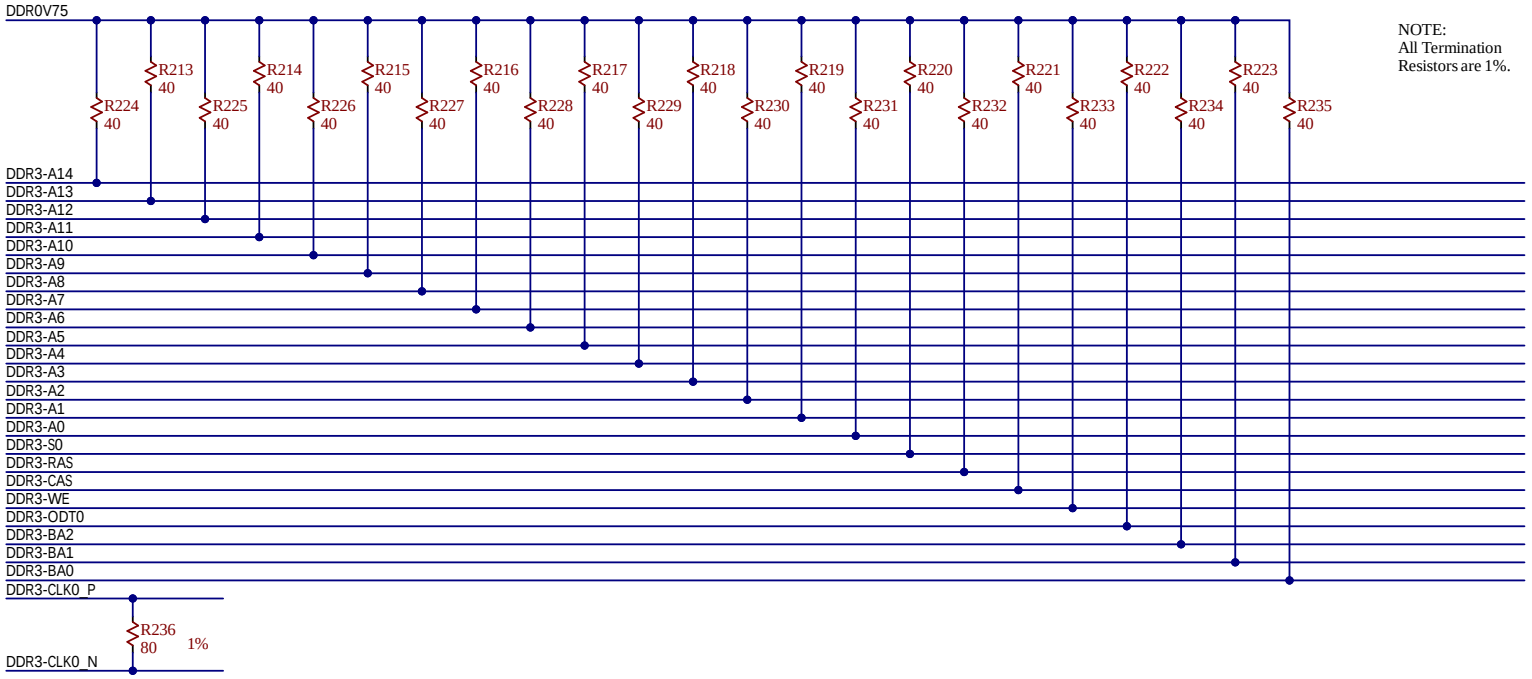
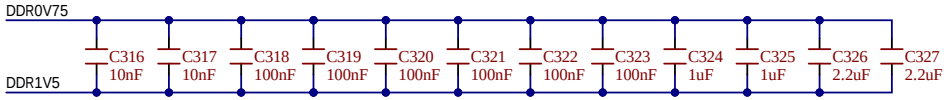
DDR3 TERMINATION



NOTE:
All Termination Resistors are 1%.



Title	ZED
Rev	F.1
Circuit	DDR3 Termination
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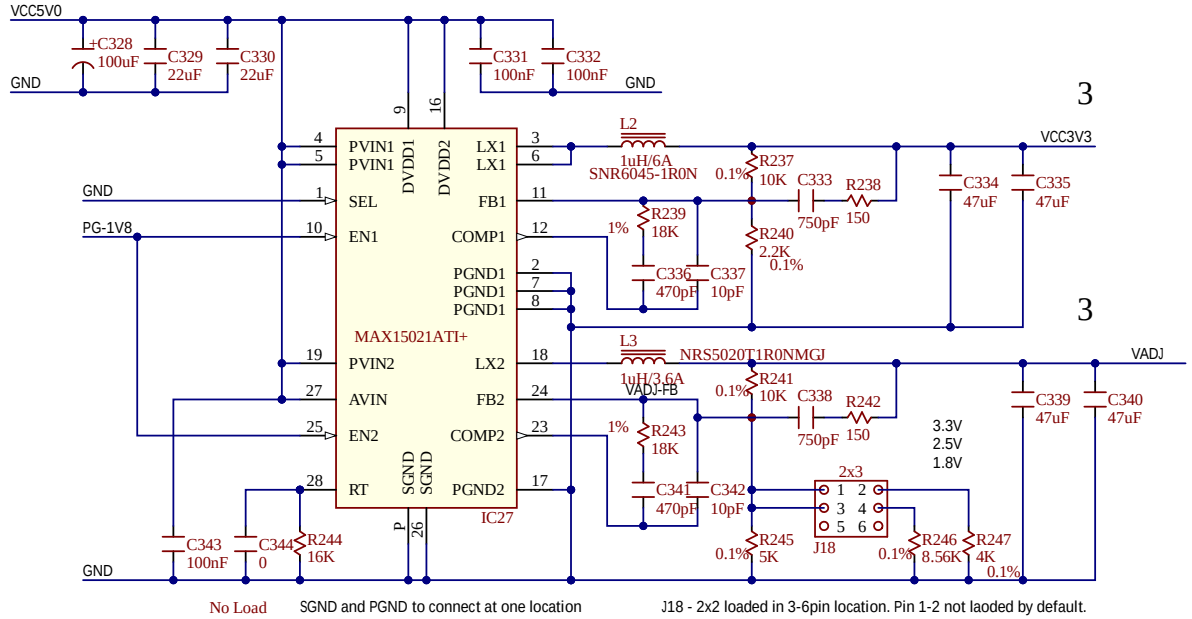

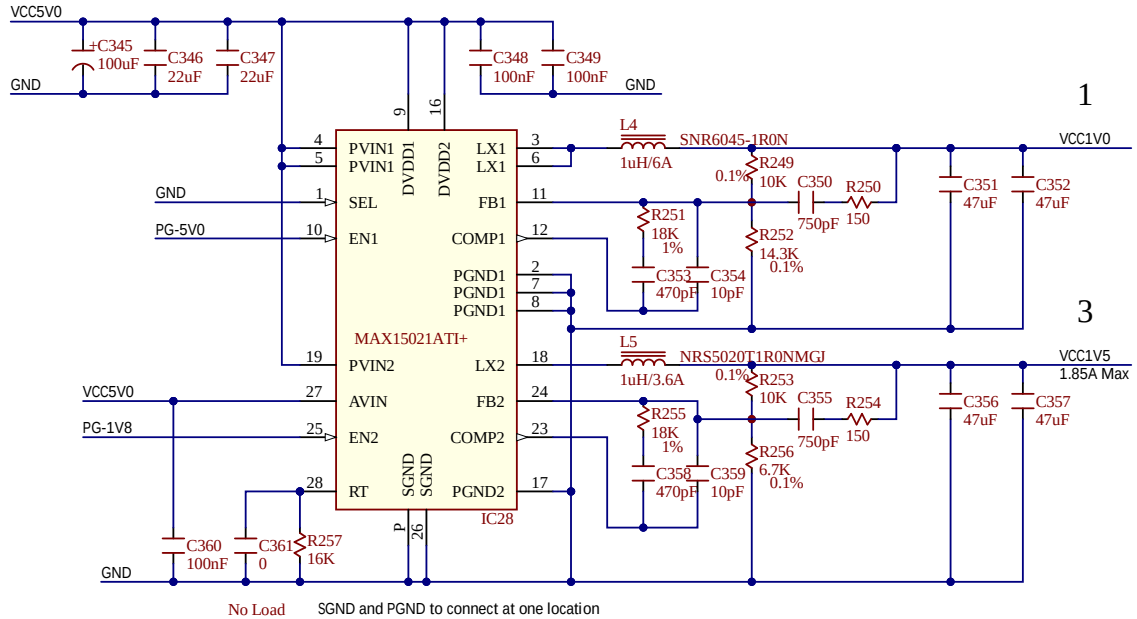

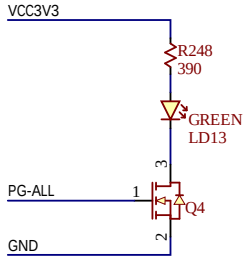

Title	ZED
Rev	F.1
Circuit	Power Regulation
Doc#	500-248
Engineer	EG
Author	GMA
Date	10/20/2020
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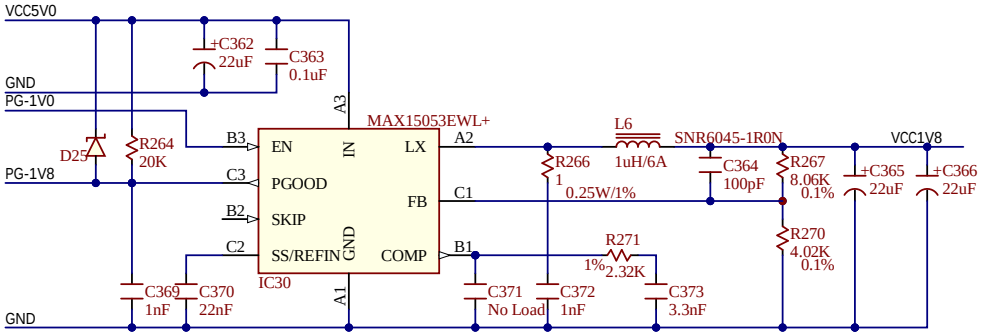
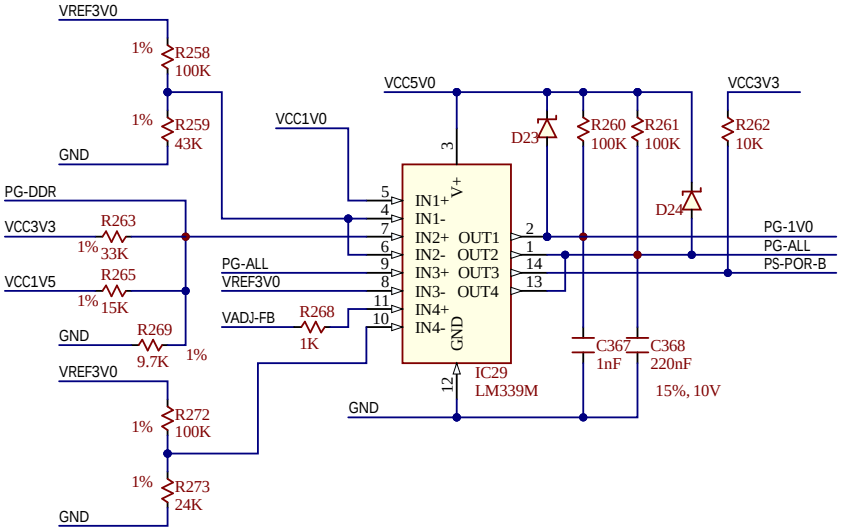
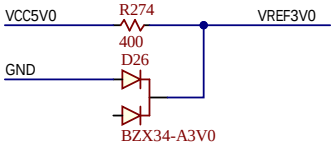
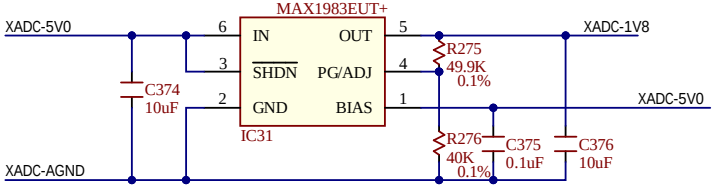
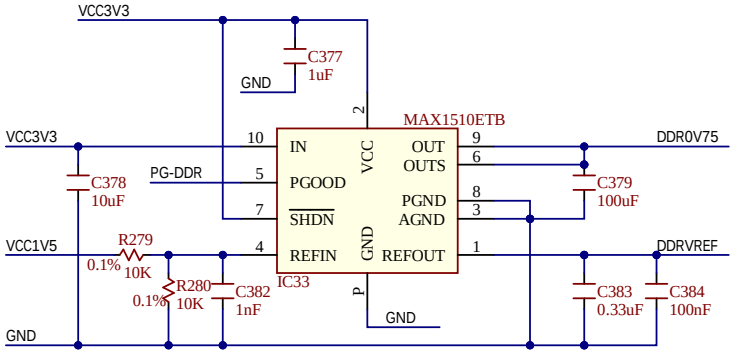


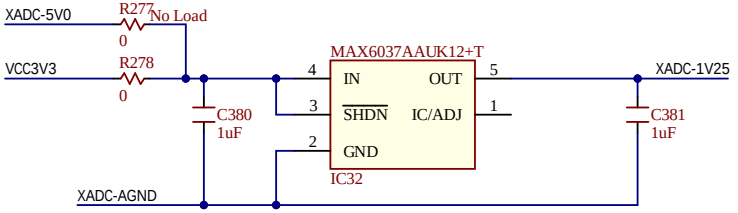
2

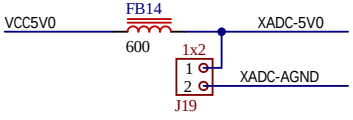


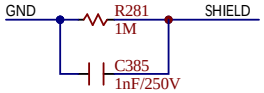












Title	ZED
Rev	F.1
Circuit	Power Regulation
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Engineer	EG
Author	GMA
Date	10/20/2020
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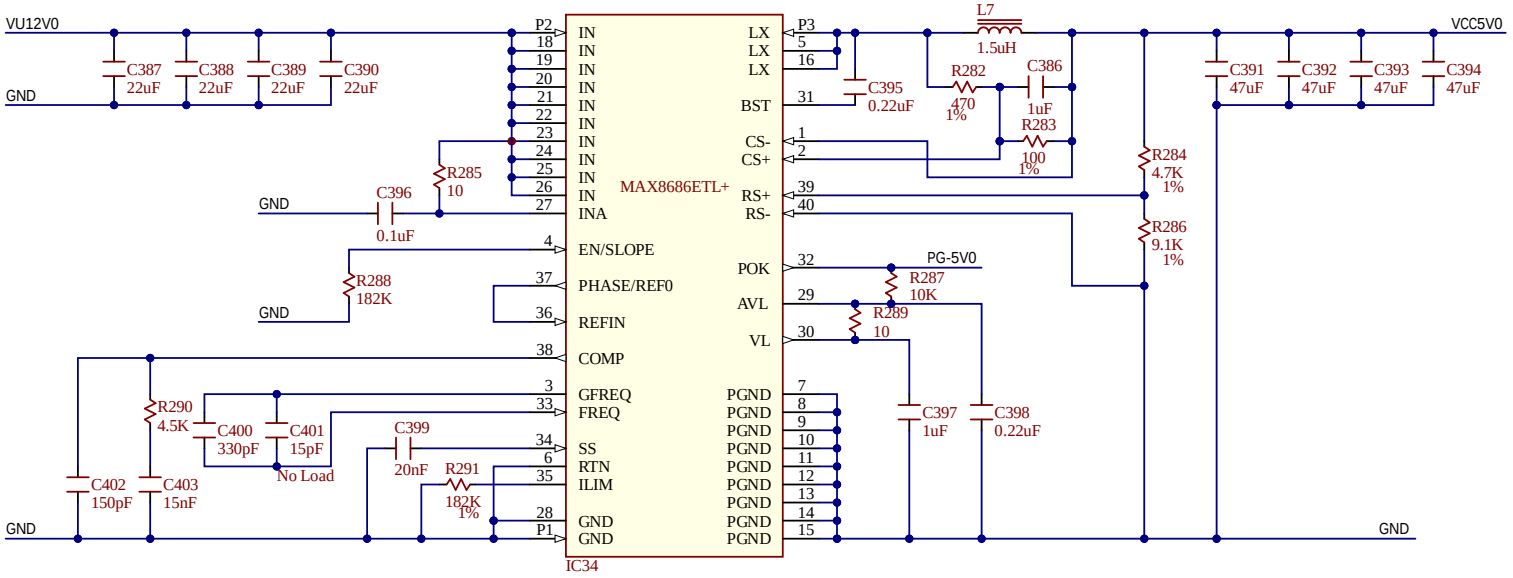

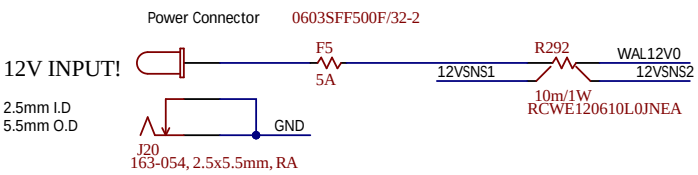

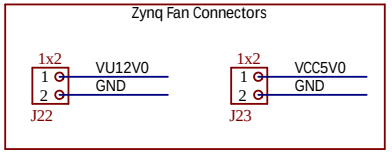

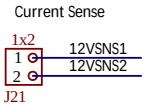

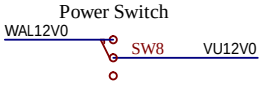

Title	ZED
Rev	F.1
Circuit	Power Regulation
Doc#	500-248
Engineer	EG
Author	GMA
Date	10/20/2020
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