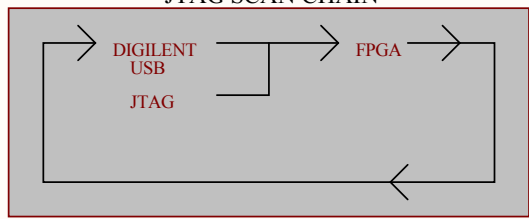
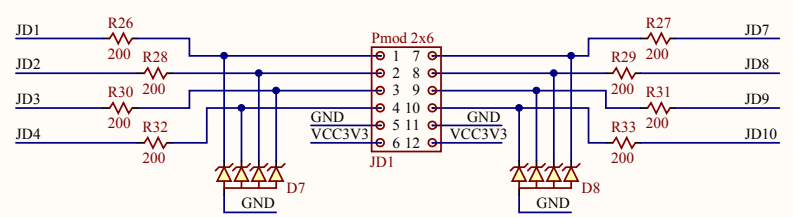
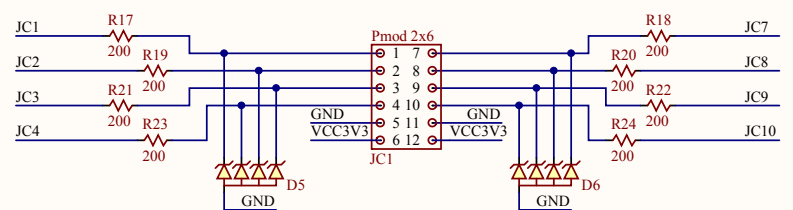
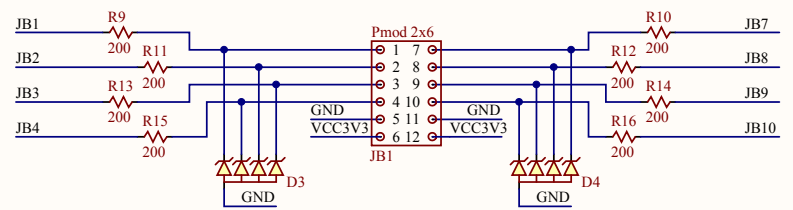
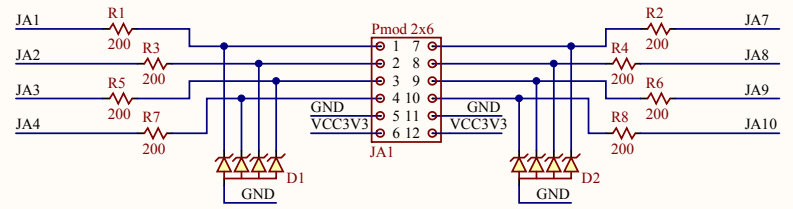


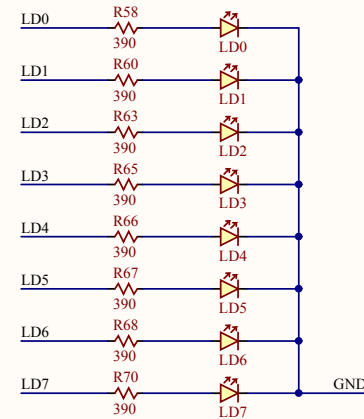
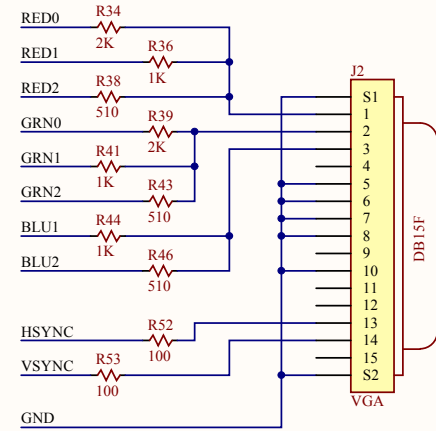
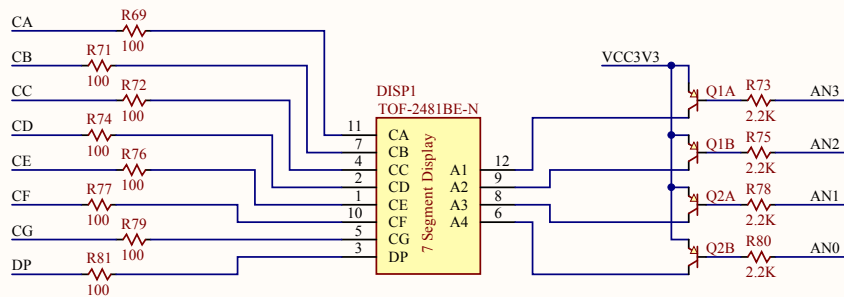
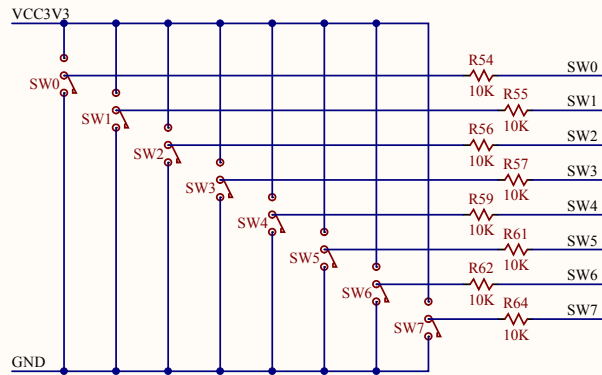
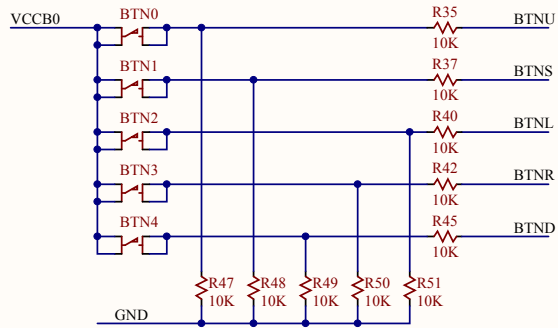
JTAG SCAN CHAIN



- Foot F1
- Foot F2
- Foot F3
- Foot F4

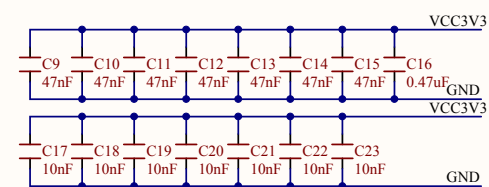
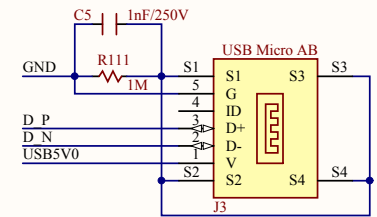
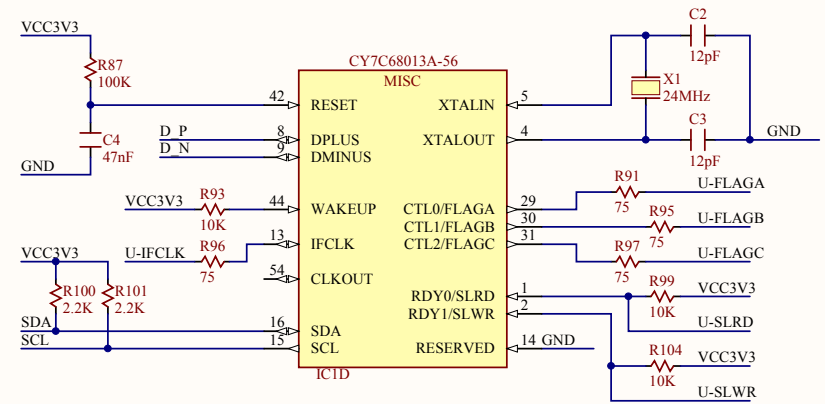
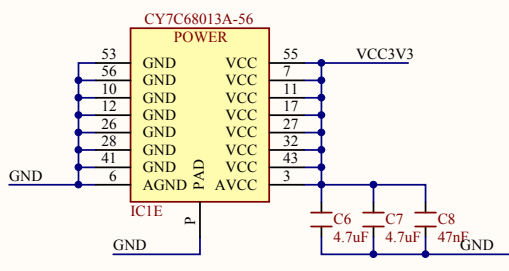
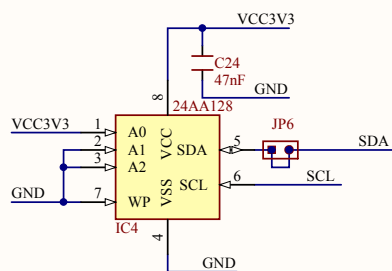
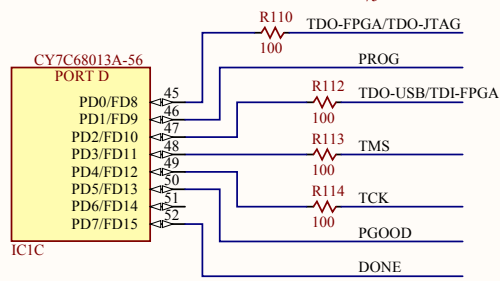
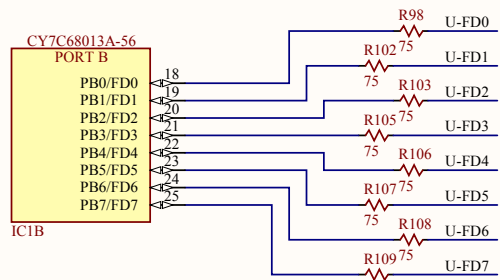
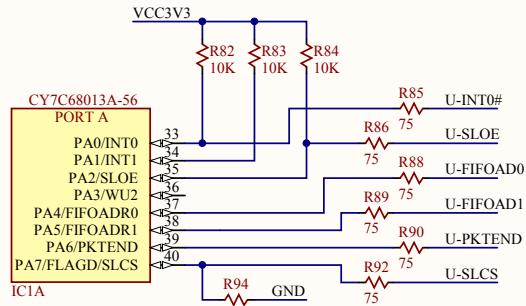


Title		Rev	
Nexys III		B.0	
Circuit		Expansion Header and IO	
Doc#		500-182	
Engineer		CC	
Author		GMA	
Date		2/17/2011	
Sheet#		1 out of 10	
		Copyright 2011	
		DIGILENT BEYOND THEORY	

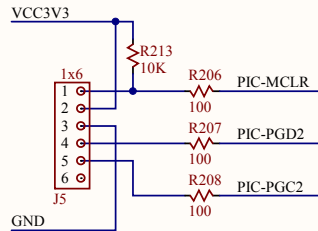
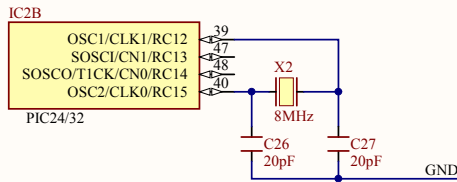
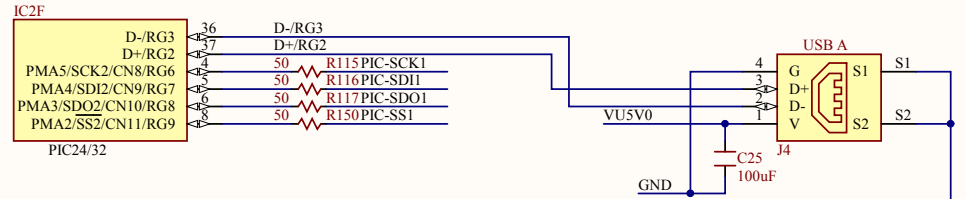
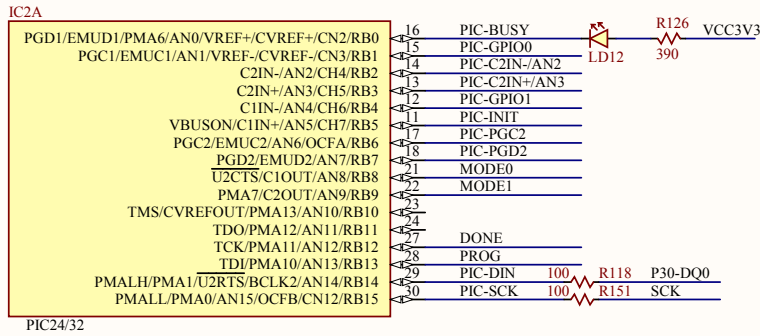


Title		Rev	
Nexys III		B.0	
Copyright 2011			
Circuit	General IO		
Doc#	500-182		
Engineer	CC		
Author	GMA		
Date	2/17/2011		
Sheet#	2 out of 10		

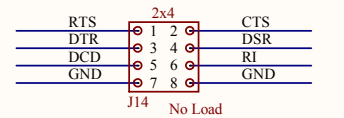
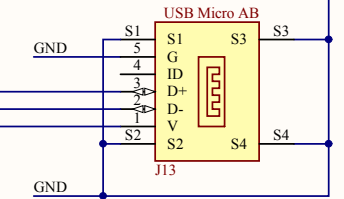
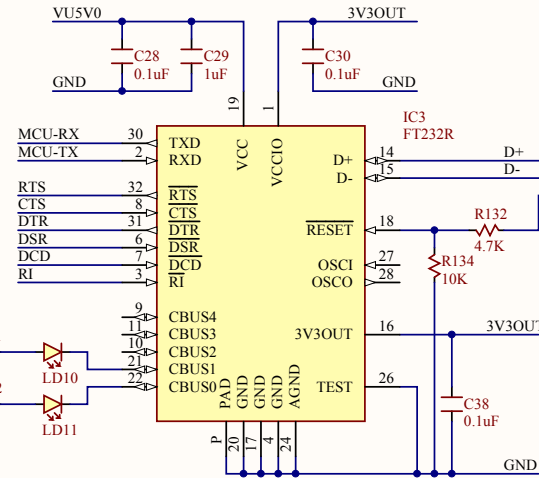
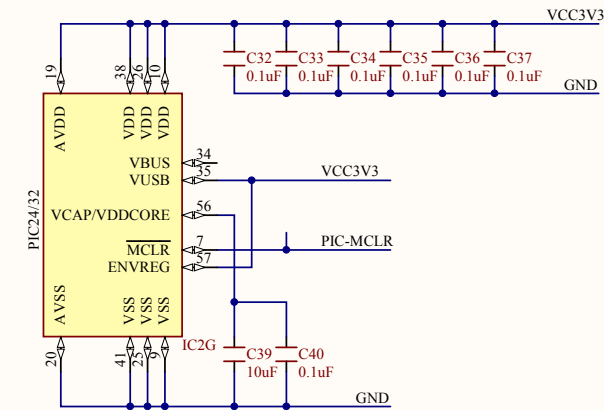
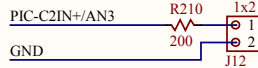
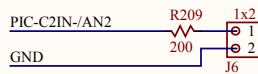




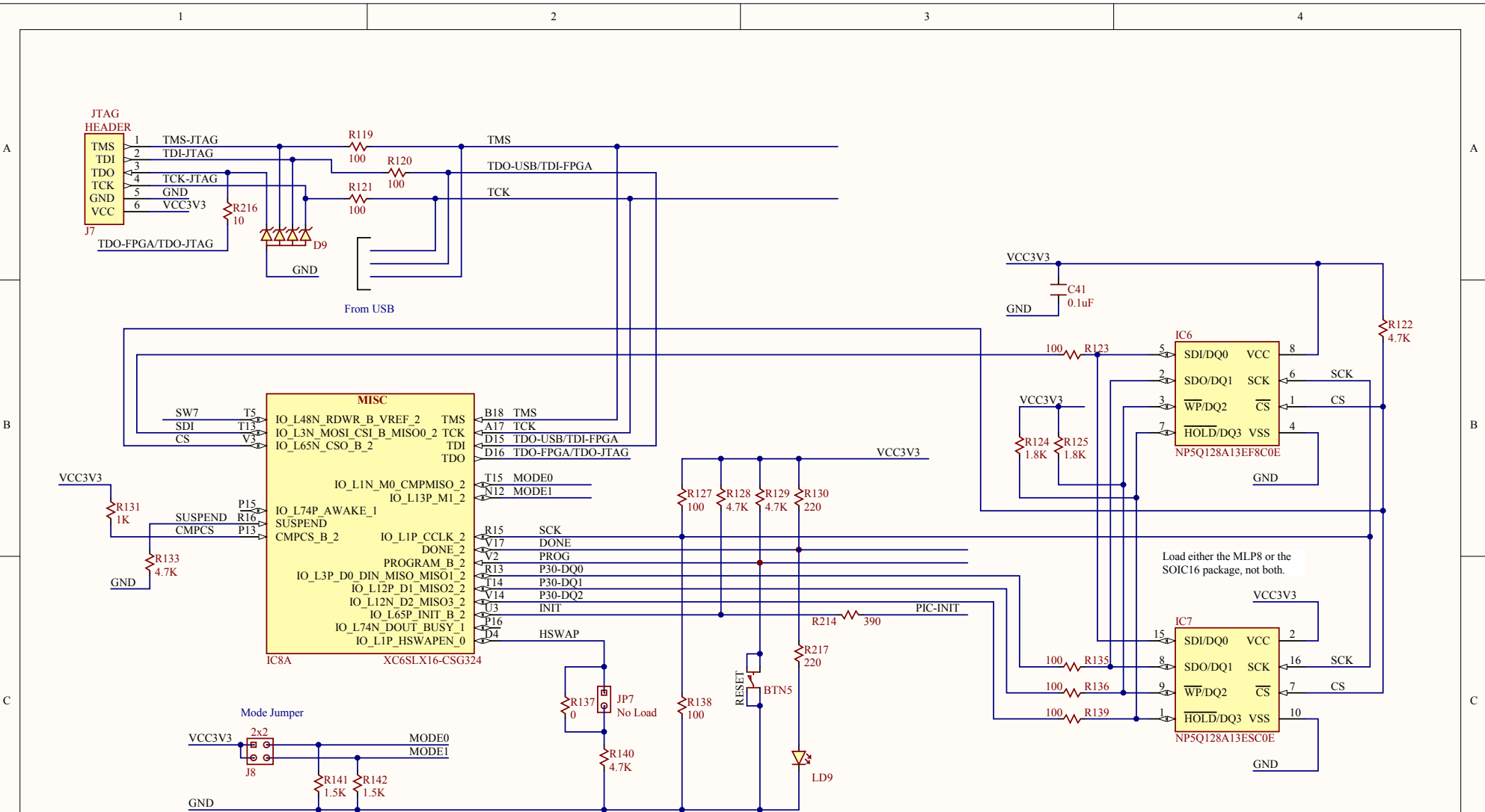
Title Nexys III		Rev B.0 Copyright 2011
Circuit USB Controller		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 3 out of 10		



ANALOG HEADERS

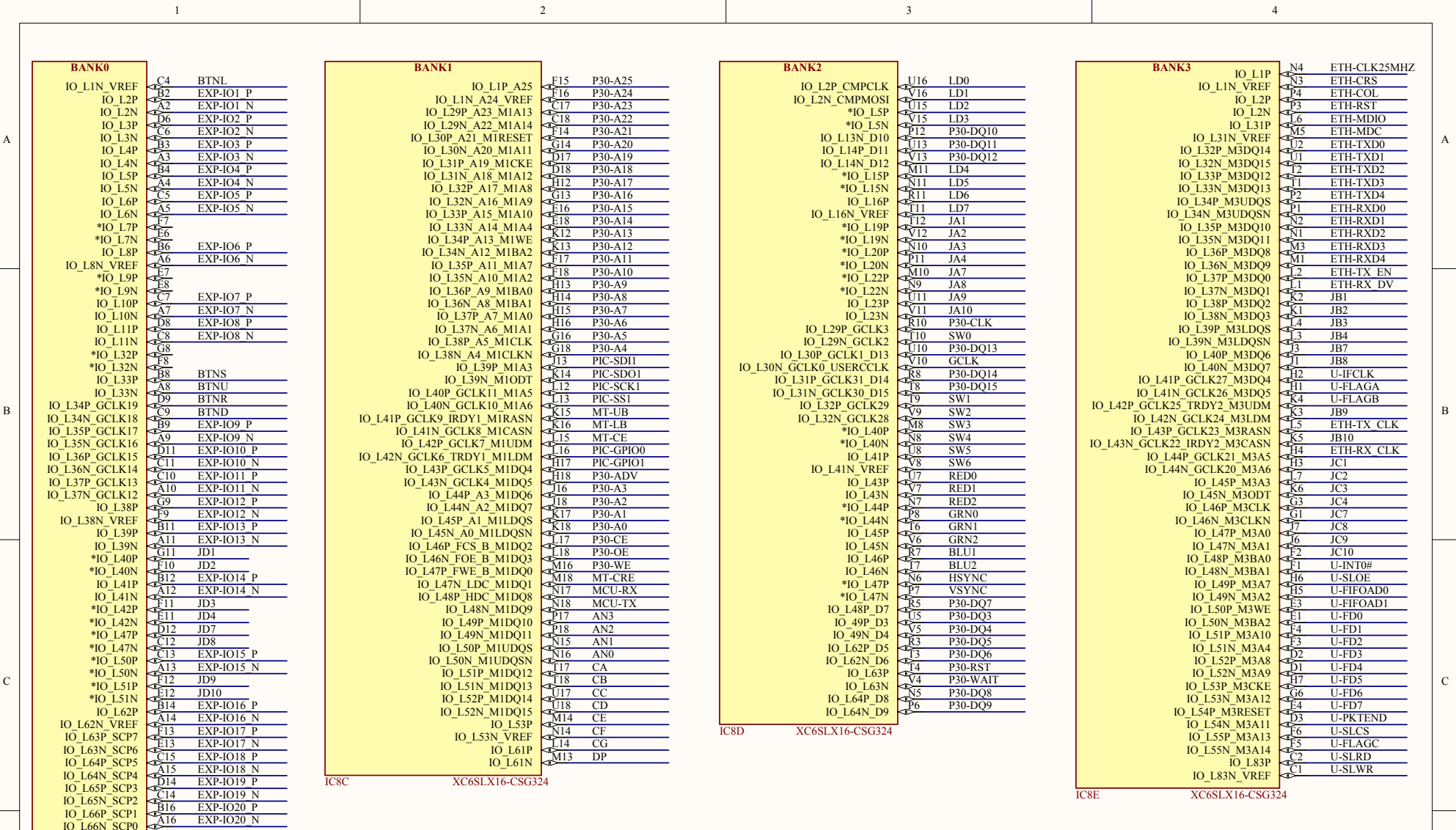


Title		Nexys III		Rev	B.0
Circuit		USB Host		Copyright 2011	
Doc#	500-182				
Engineer	CC				
Author	GMA				
Date	2/17/2011				
Sheet#	4 out of 10				

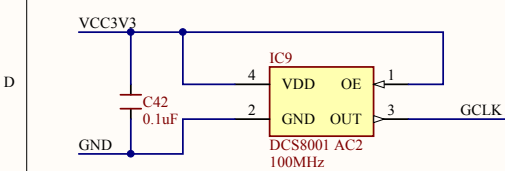


M1	M0	Configuration Mode
0	0	BPI
0	1	SPI - On Board SPI Flash
1	0	-----
1	1	Slave Serial - USB Memory

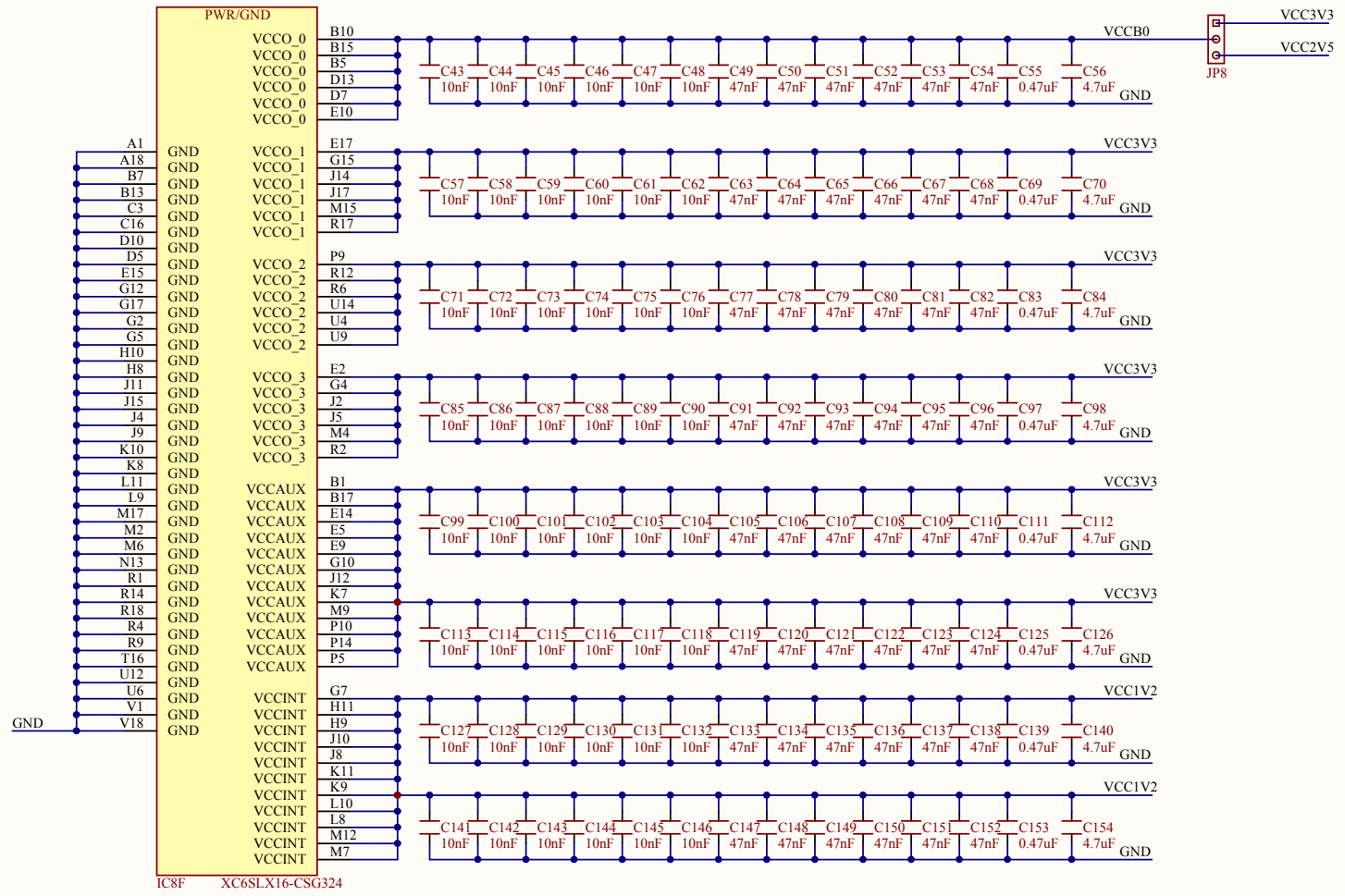
Title		<h1>Nexys III</h1>	Rev	B.0 Copyright 2011
Circuit			Configuration	
Doc#		500-182		
Engineer		CC		
Author		GMA		
Date		2/17/2011		
Sheet#		5 out of 10		



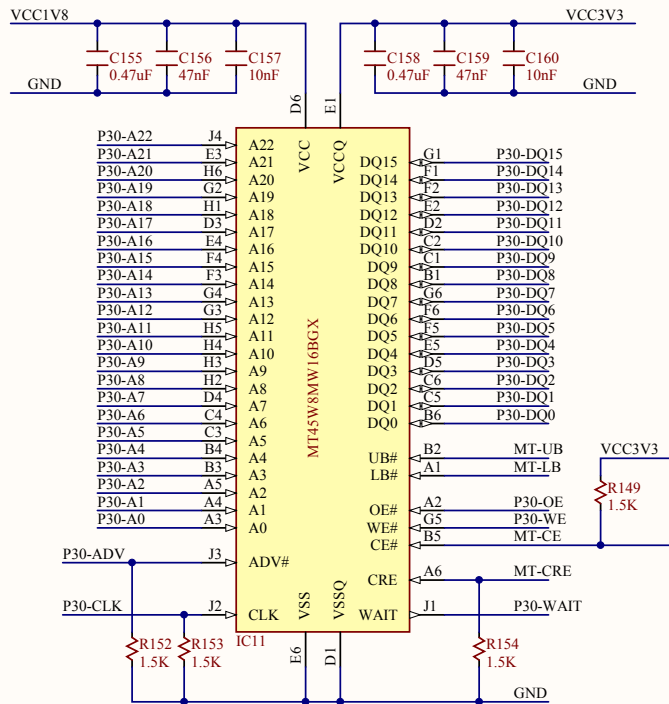
IC8B XC6SLX16-CSG324
 NOTE: * = LX16 Die only (except L50) on Bank 0



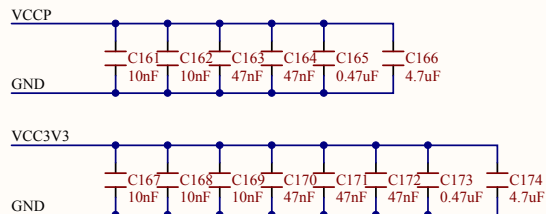
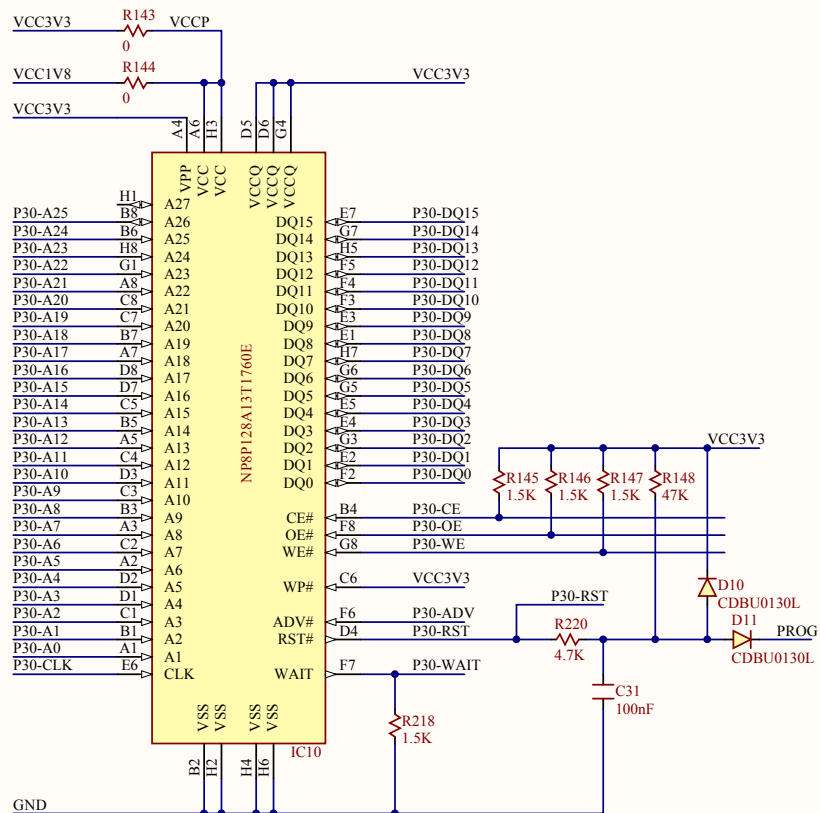
Title Nexys III		Rev B.0 Copyright 2011
Circuit SPARTAN 6		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 6 out of 10		




Title		Nexys III		Rev		B.0	
Circuit		Spartan 6 Power		Copyright		2011	
Doc#		500-182					
Engineer		CC					
Author		GMA					
Date		2/17/2011					
Sheet#		7 out of 10					



Note: Load resistor to 3.3V and remove resistor to 1.8V for P33

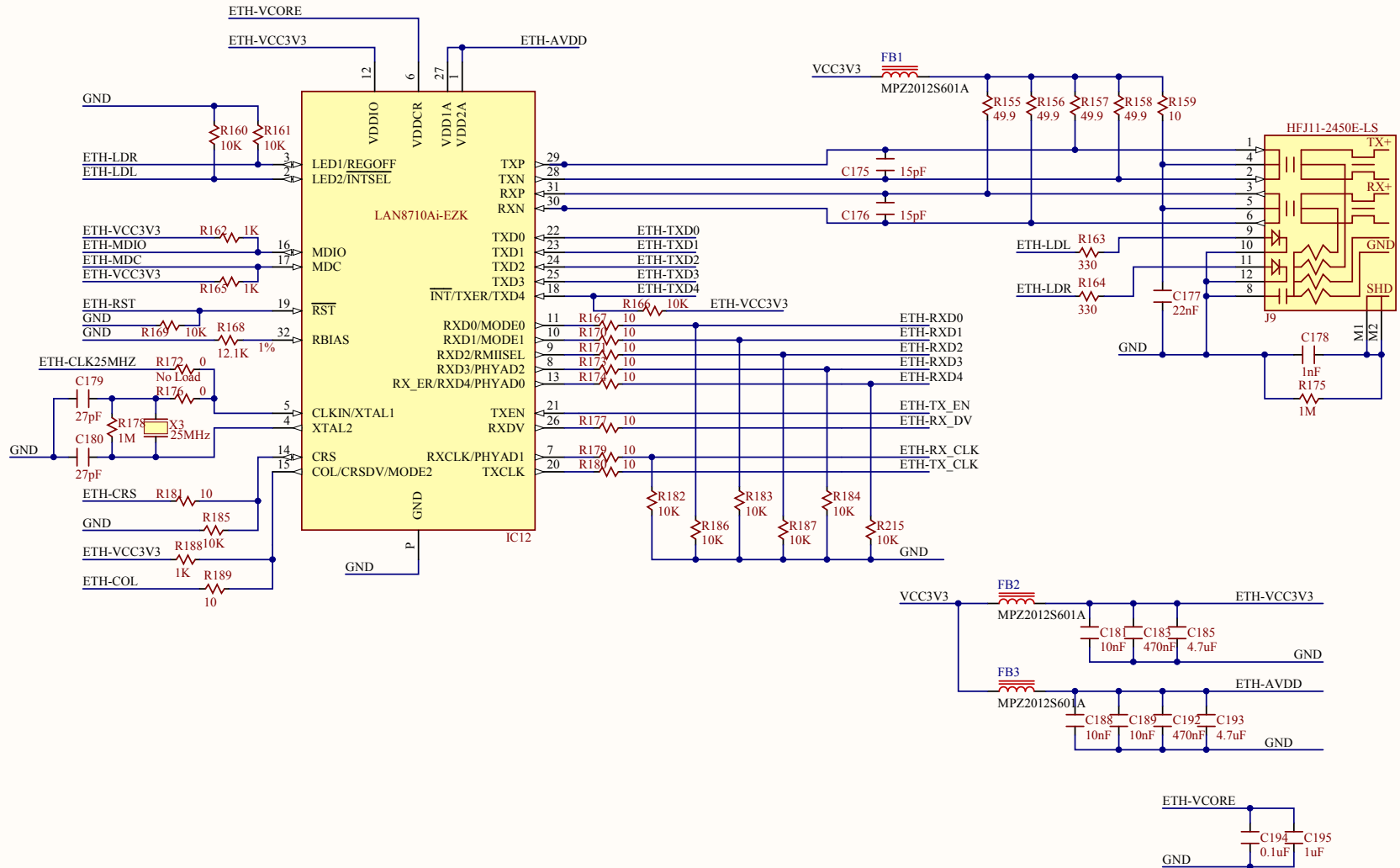



Title		Rev	
<h1>Nexys III</h1>		<h1>B.0</h1>	
		Copyright 2011	
Circuit	Memory		
Doc#	500-182		
Engineer	CC		
Author	GMA		
Date	2/17/2011		
Sheet#	8 out of 10		

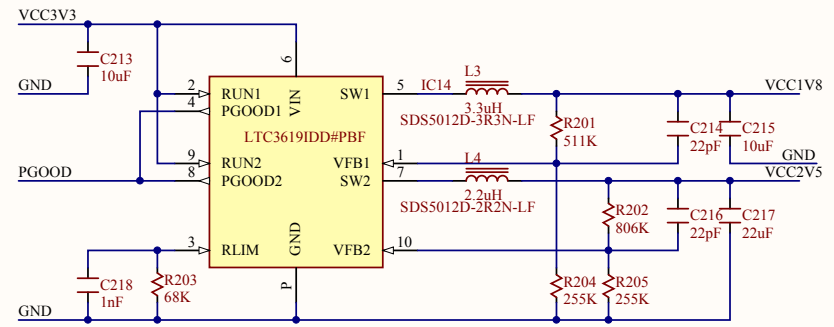
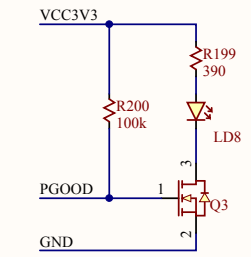
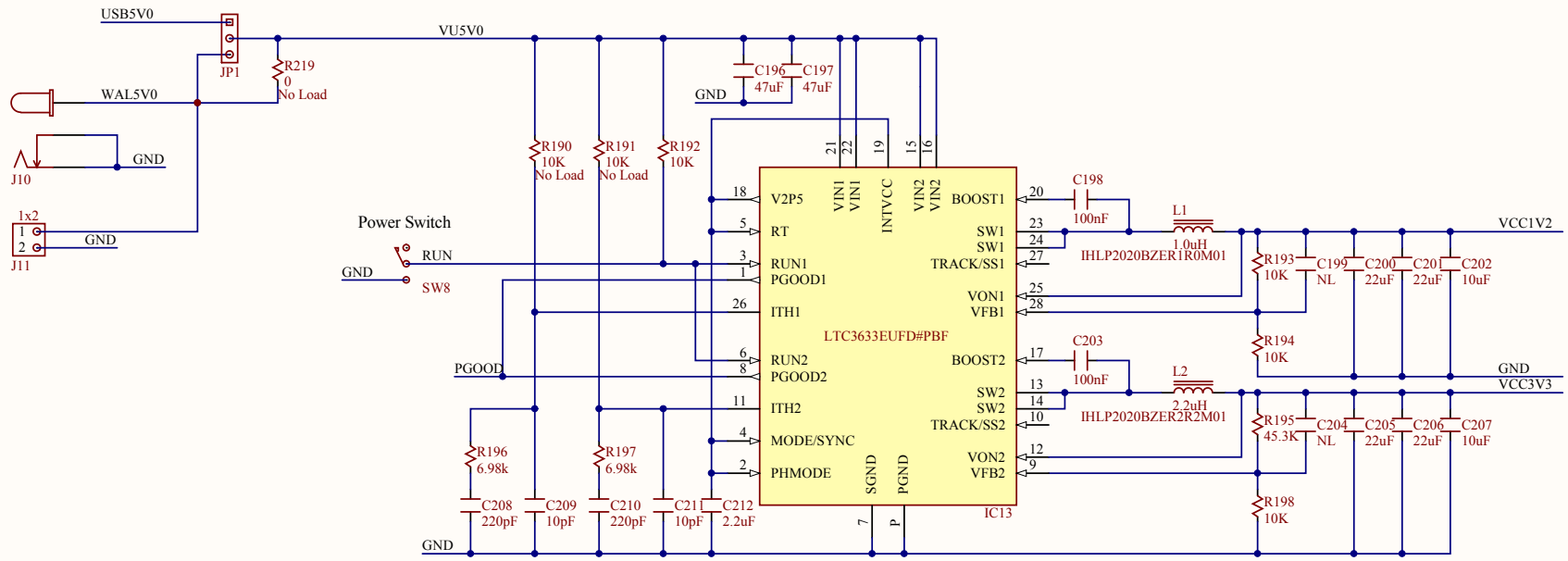


DIGILENT
BEYOND THEORY

ETHERNET



Title <h2 style="margin: 0;">Nexys III</h2>		Rev B.0 Copyright 2011
Circuit Ethernet		
Doc# 500-182		
Engineer CC		
Author GMA		
Date 2/17/2011		
Sheet# 9 out of 10		



Title		Nexys III		Rev		B.0	
Circuit		Power		Copyright		2011	
Doc#		500-182					
Engineer		CC					
Author		GMA					
Date		2/17/2011					
Sheet#		10 out of 10					