

- CE
- ROHS
- Xilinx
- Digilent Inc.
- Chinese ROHS
- Analog Devices

- F1 Foot
- F2 Foot
- F3 Foot
- F4 Foot

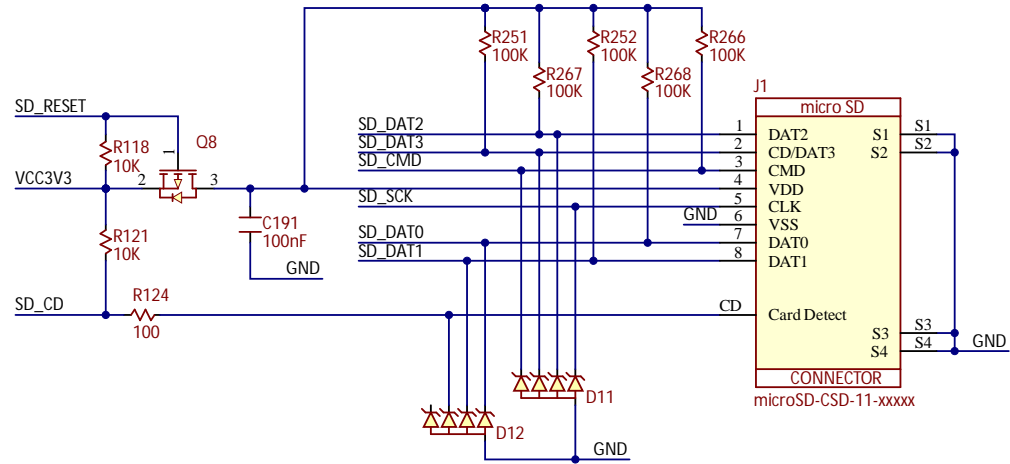
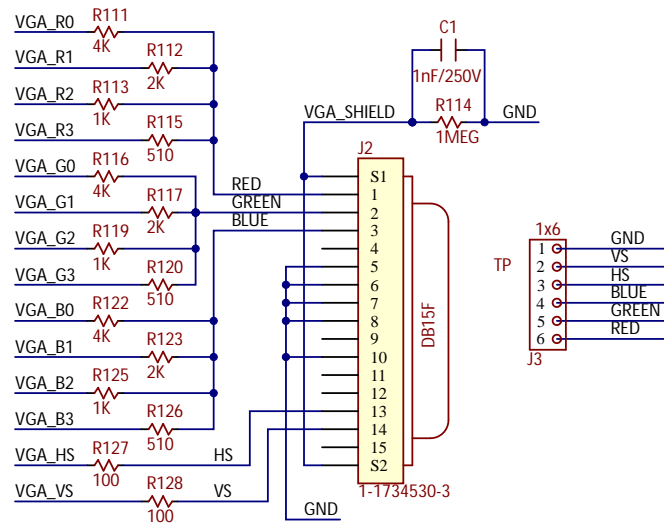
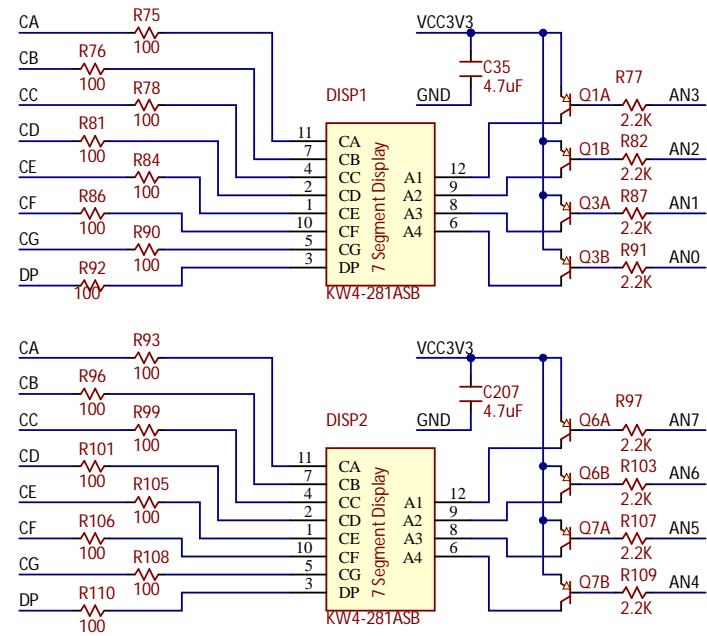
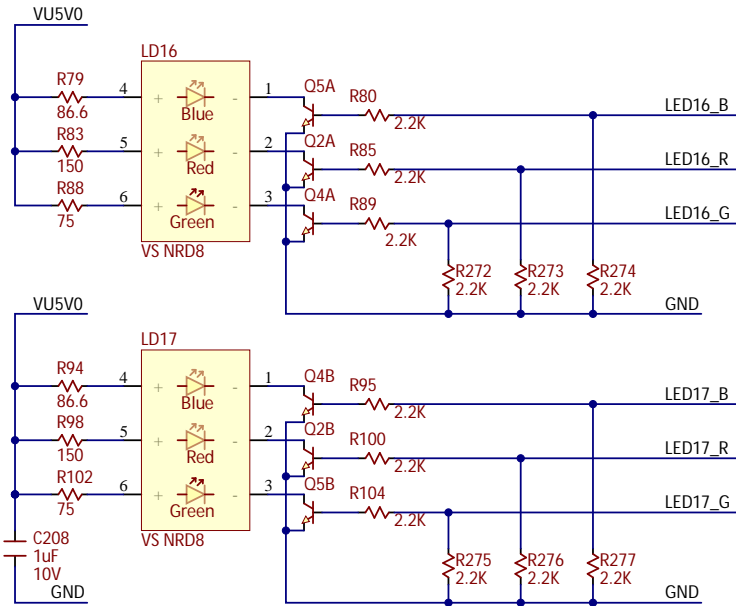
Title		Rev
Nexys A7		D.3
Circuit		
PMD0_10		
Doc# 500-292		
Engineer EG		
Author DL		
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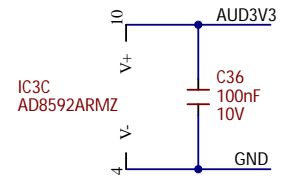
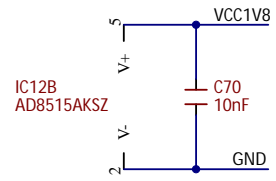
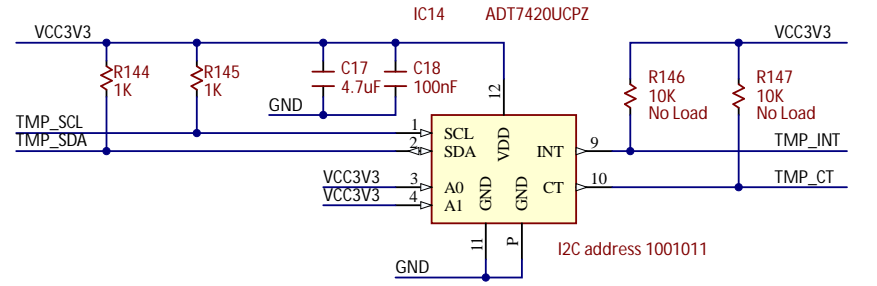
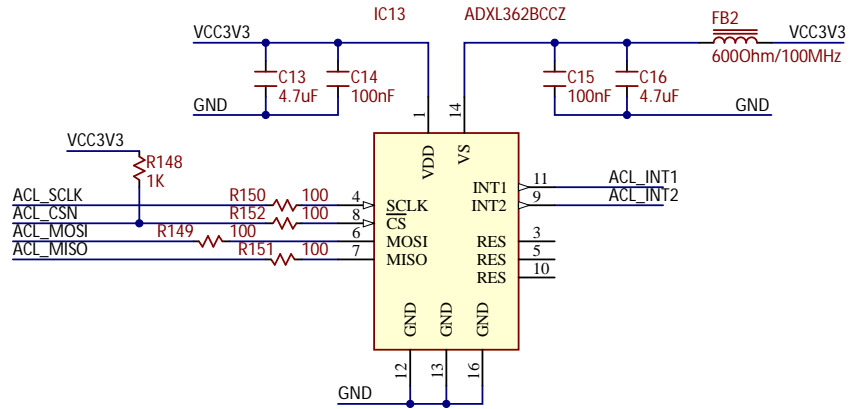
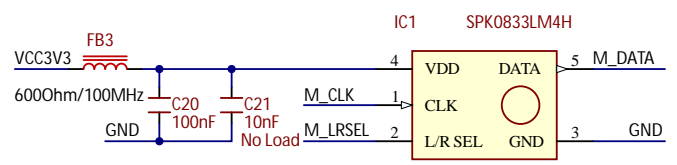
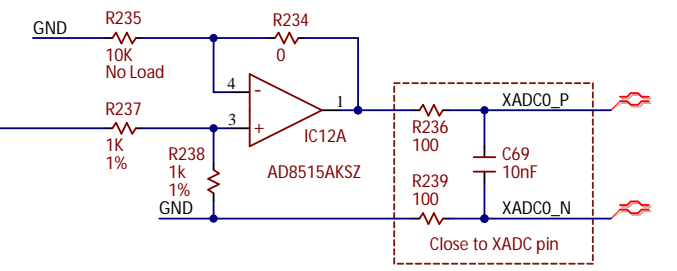
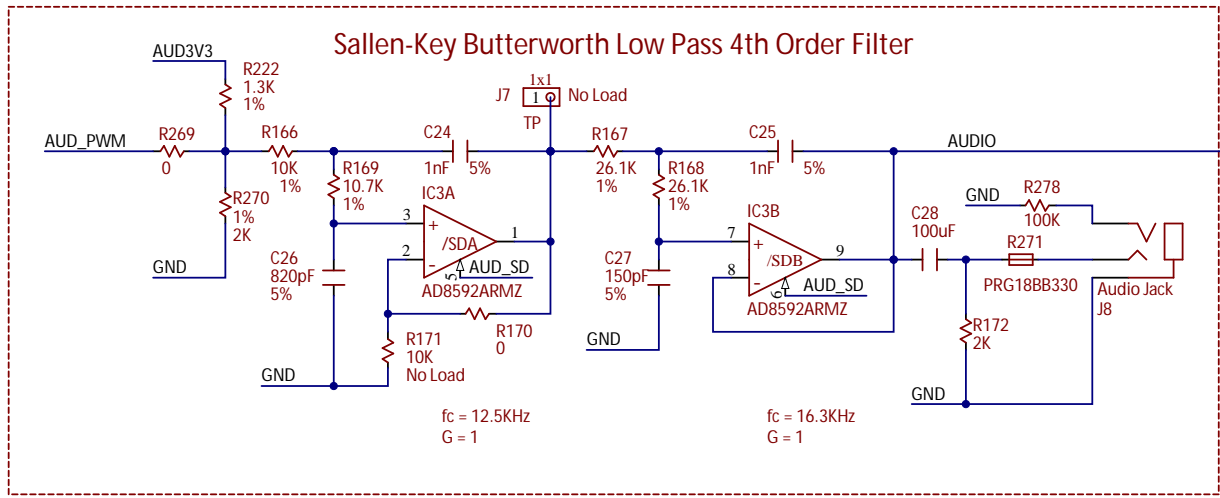


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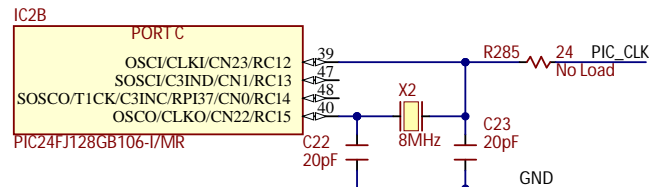
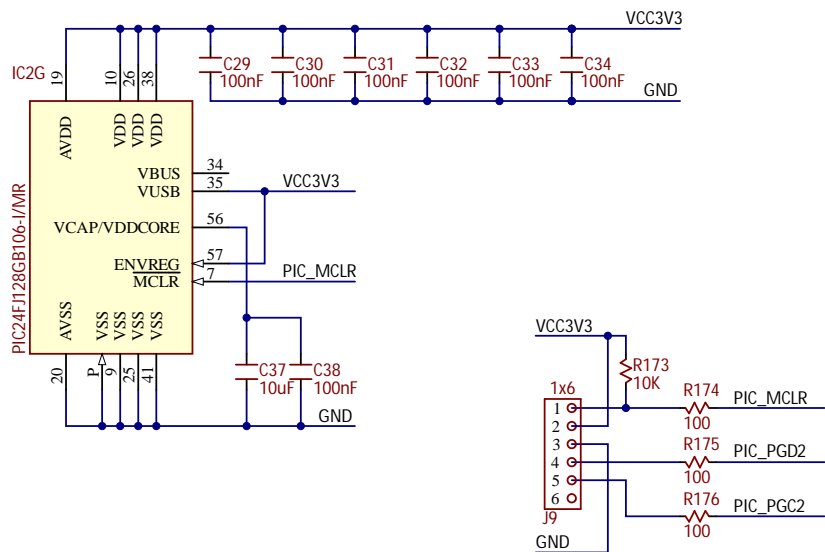
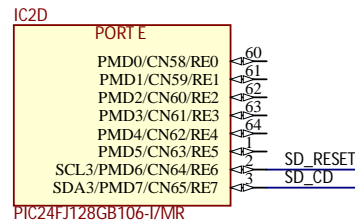
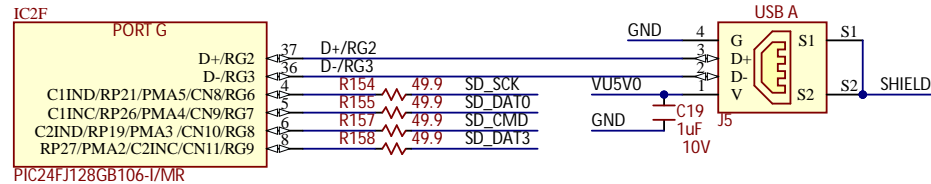
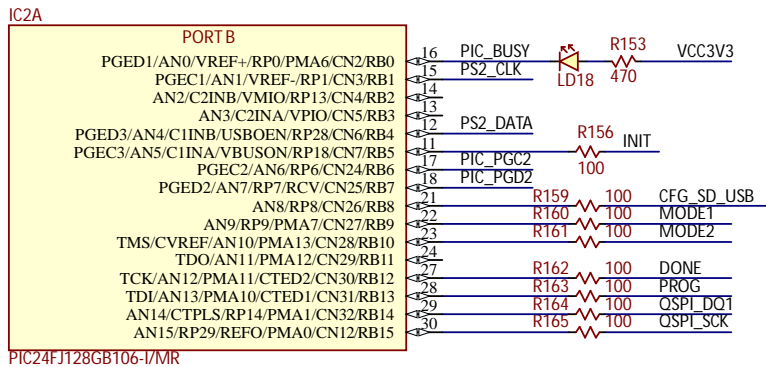




For more information on the parts used in this design, please refer to:

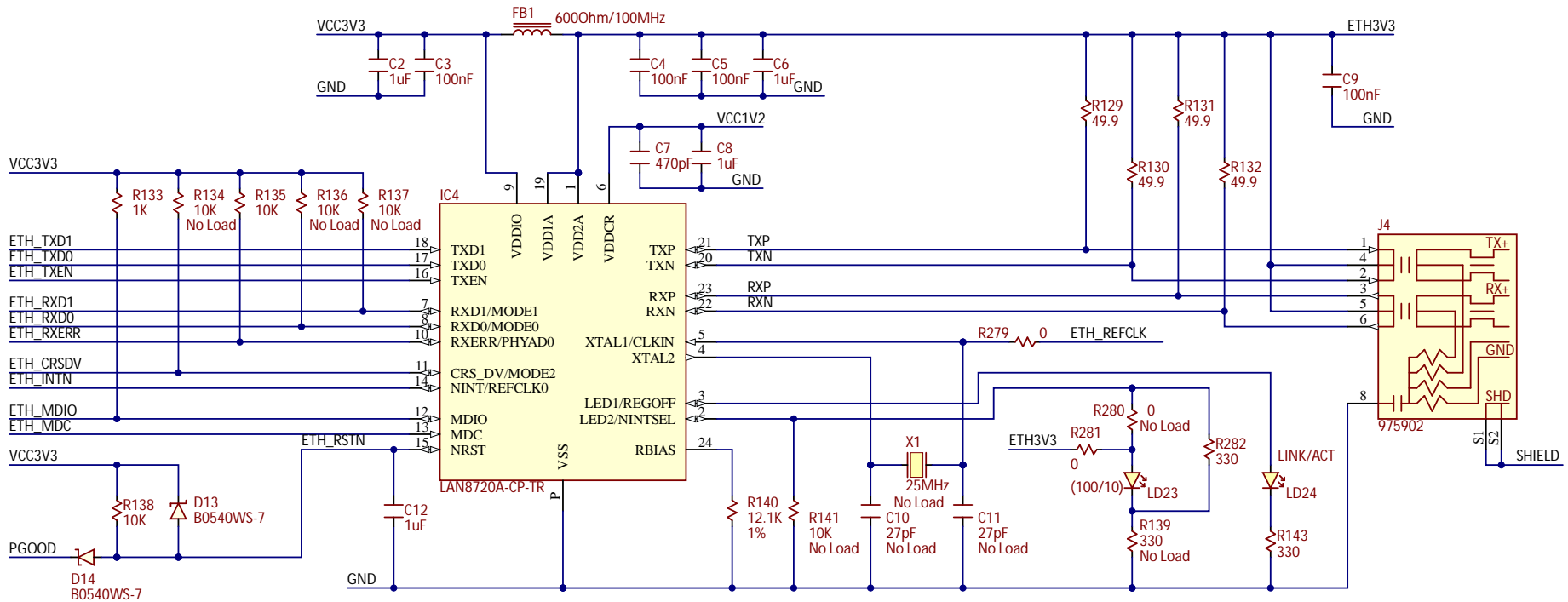
- <http://www.analog.com/ad8592> (CMOS Single Supply RRIO Dual Op Amp with ±250 mA Output Current and Shutdown Mode)
- <http://www.analog.com/ad8515> (1.8 V Low Power CMOS Rail-to-Rail Input/Output Operational Amplifier)
- <http://www.analog.com/adxl362> (Micropower, 3-Axis, ±2 g/±4 g/±8 g Digital Output MEMS Accelerometer)
- <http://www.analog.com/adt7420> (±0.25°C Accurate, 16-Bit Digital I2C Temperature Sensor)

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USB HID			
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NOTE: REF_CLK In Mode (ETH_REFCLK = 50MHz)

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ETHERNET		
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1

2

3

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A

A

B

B

C

C

D

D

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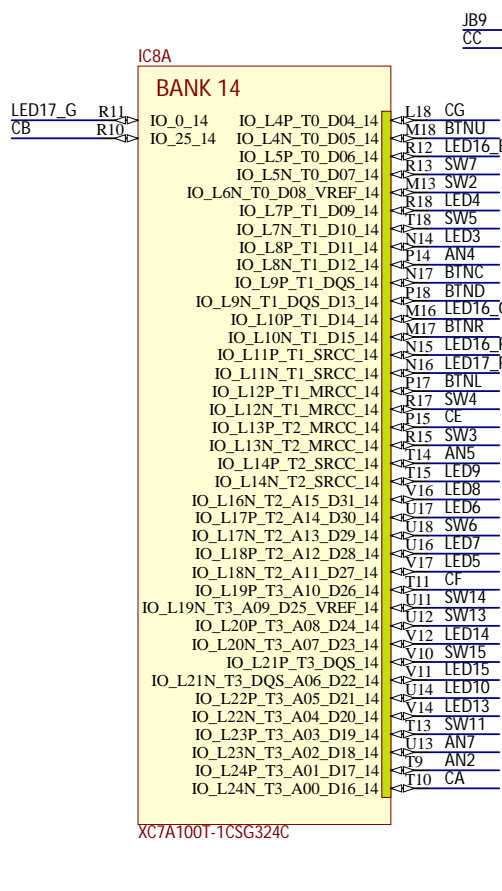
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2

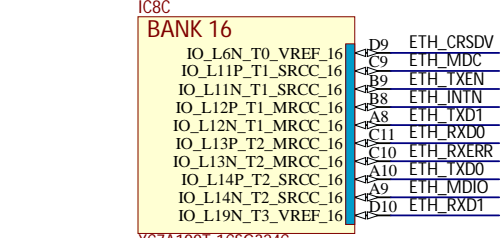
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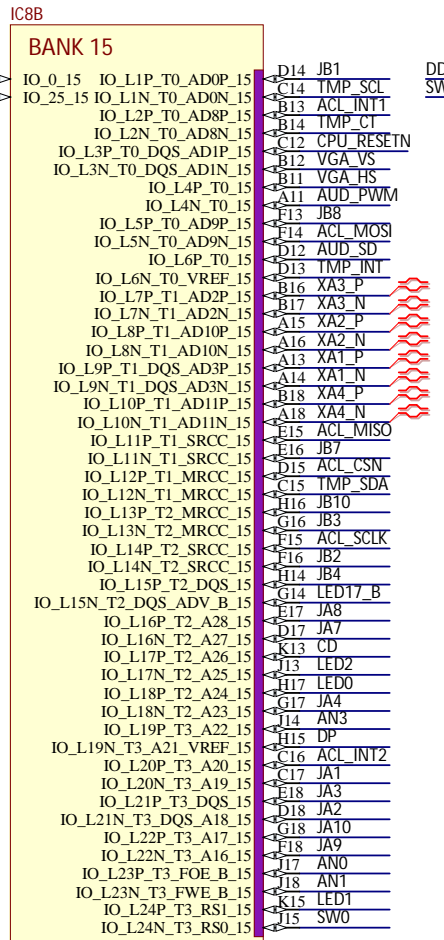
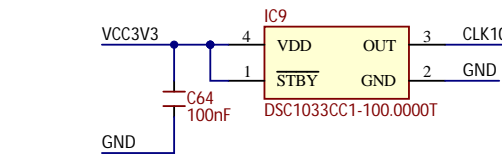
For the -50T variant: IC8=XC7A50T-1CSG324I



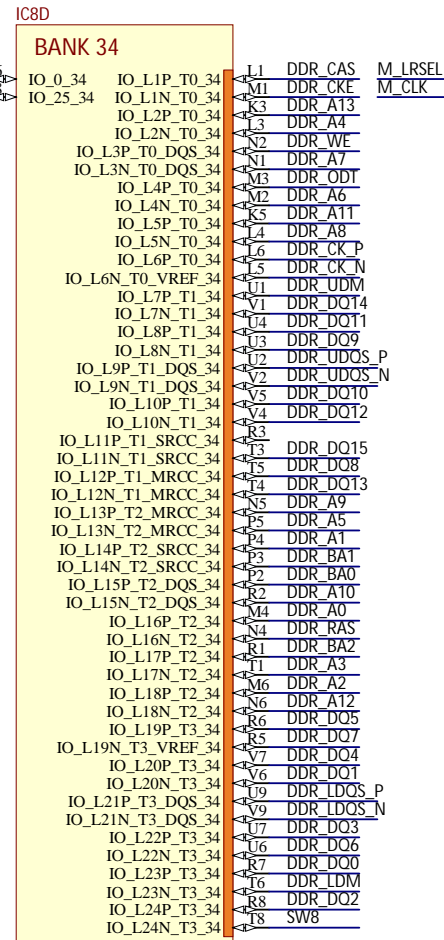
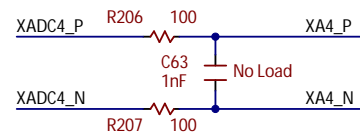
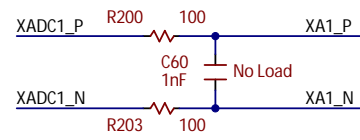
XC7A100T-1CSG324C



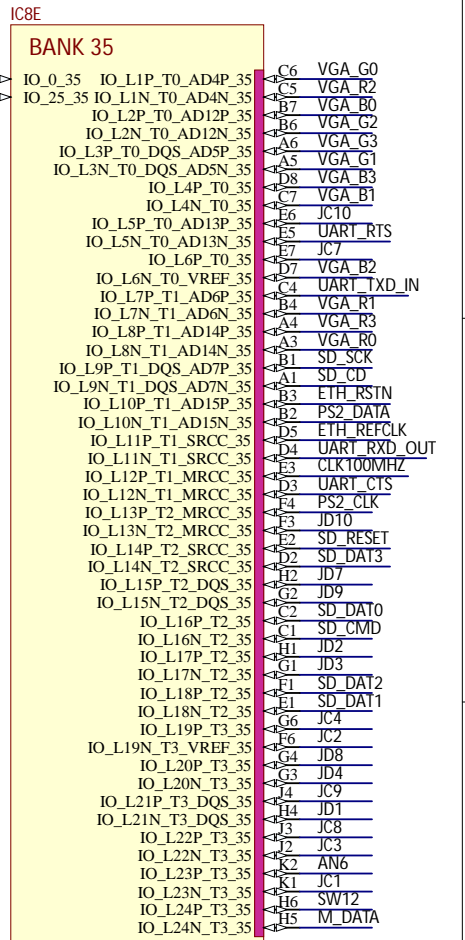
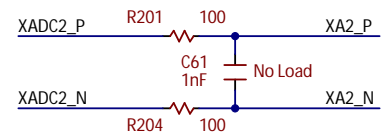
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XC7A100T-1CSG324C

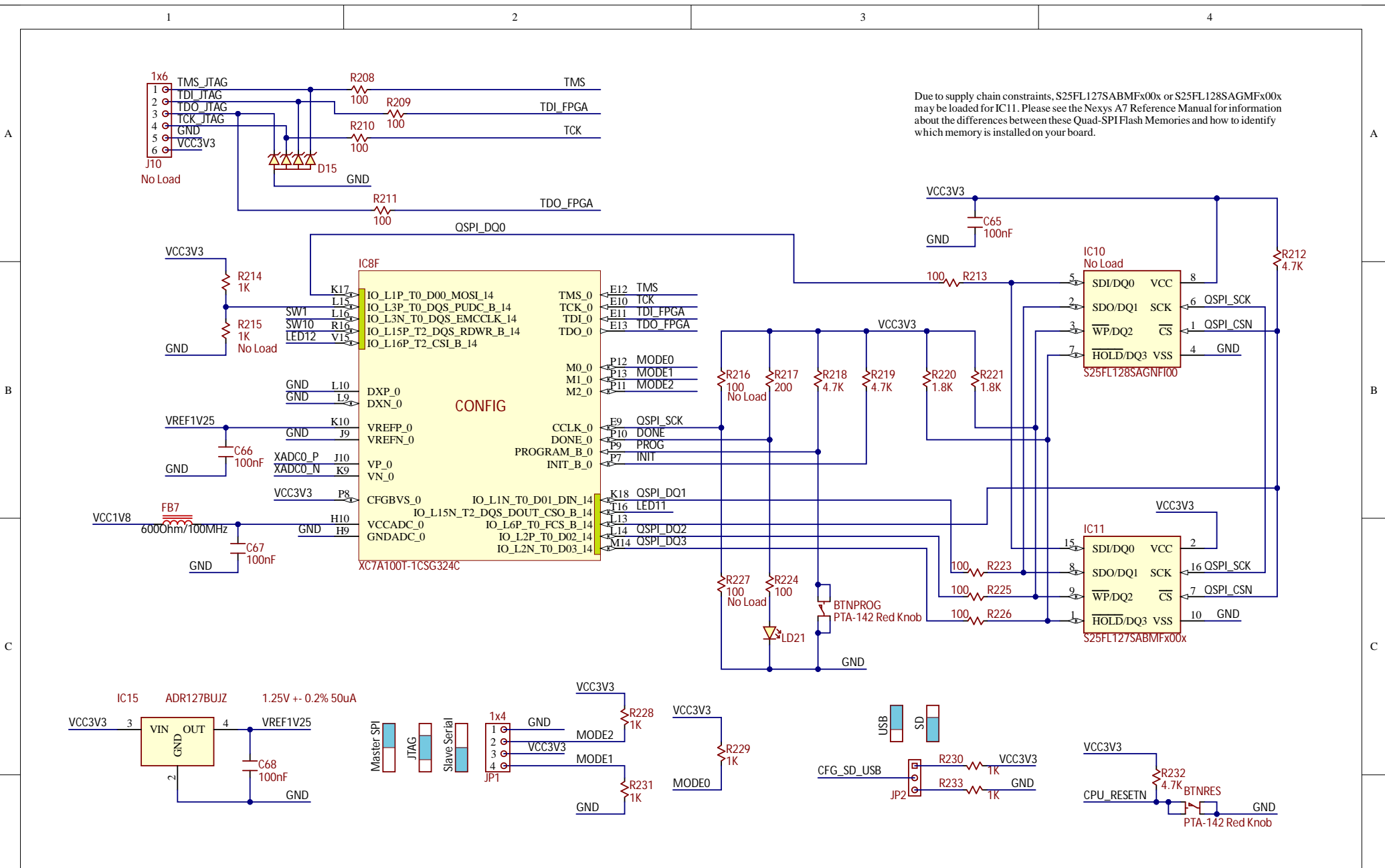


XC7A100T-1CSG324C



XC7A100T-1CSG324C

Title Nexys A7		Rev D.3
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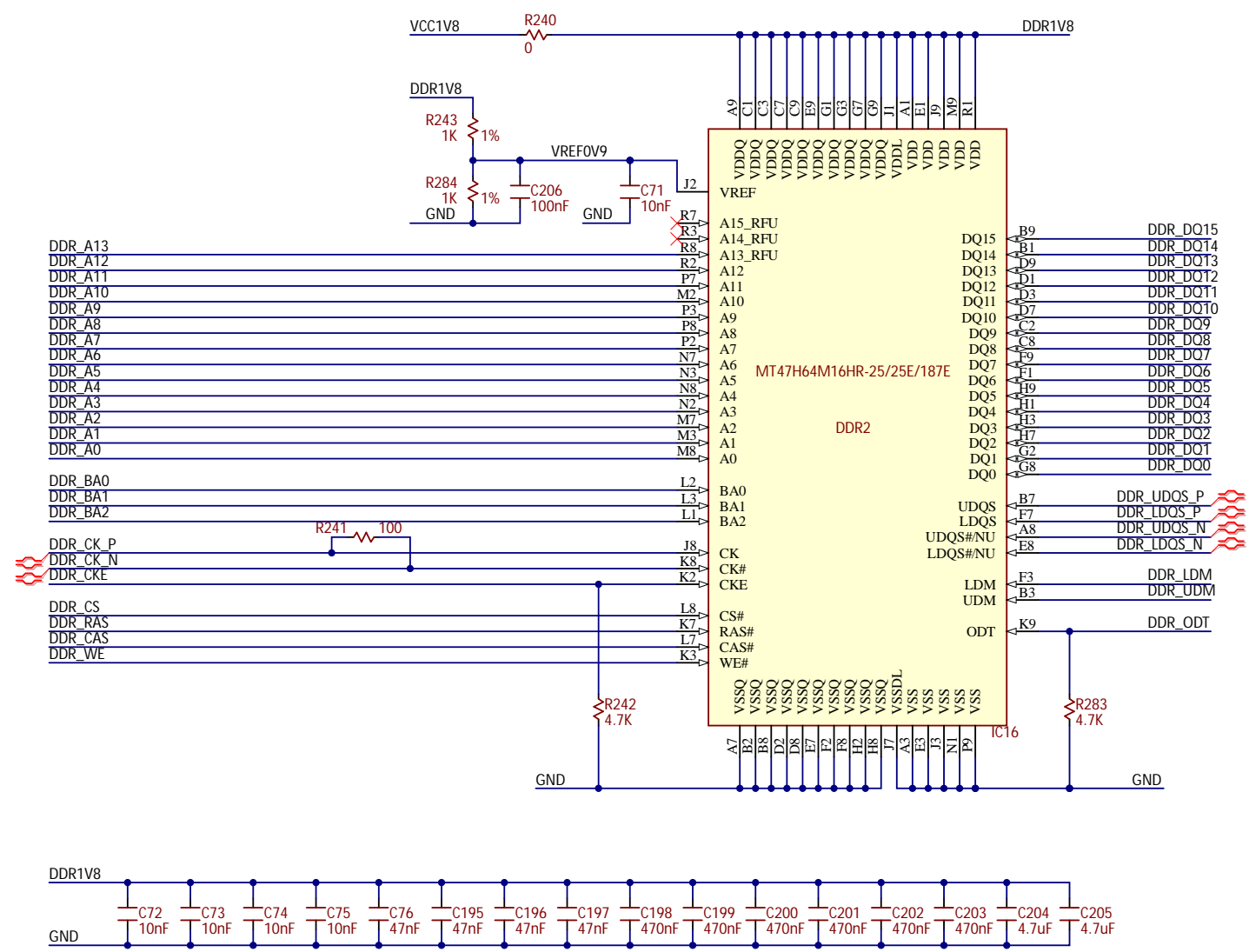
Due to supply chain constraints, S25FL127SABMFx00x or S25FL128SAGMFx00x may be loaded for IC11. Please see the Nexys A7 Reference Manual for information about the differences between these Quad-SPI Flash Memories and how to identify which memory is installed on your board.

For more information on the parts used in this design, please refer to:
<http://www.analog.com/adr127> (Precision, Micropower LDO Voltage References in TSOT)

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CONFIG, SPIFLASH			
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Circuit		DDR2 Memory		Doc#		500-292	
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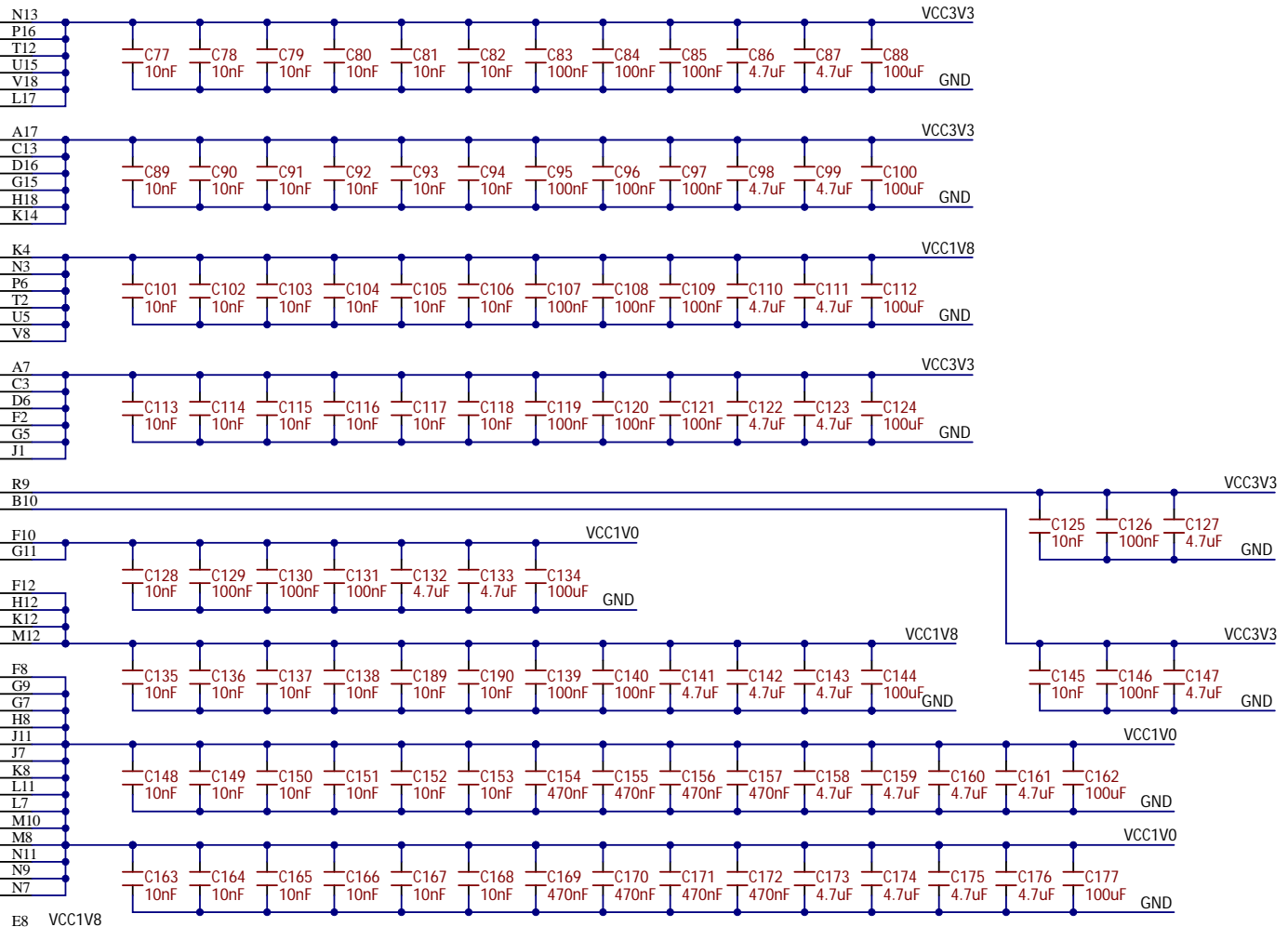
IC8G

PWR/GND

- A12 GND
- A2 GND
- B15 GND
- B5 GND
- C18 GND
- C8 GND
- D11 GND
- D1 GND
- E14 GND
- E4 GND
- F17 GND
- F11 GND
- F9 GND
- F7 GND
- G12 GND
- G10 GND
- G8 GND
- H13 GND
- H11 GND
- H7 GND
- H3 GND
- J16 GND
- J12 GND
- J8 GND
- J6 GND
- K11 GND
- K7 GND
- L12 GND
- L8 GND
- L2 GND
- M15 GND
- M11 GND
- M9 GND
- M7 GND
- M5 GND
- N18 GND
- N12 GND
- N10 GND
- N8 GND
- P1 GND
- R14 GND
- R4 GND
- T7 GND
- U10 GND
- V13 GND
- V3 GND

- VCCO_14 N13
- VCCO_14 P16
- VCCO_14 T12
- VCCO_14 U15
- VCCO_14 V18
- VCCO_14 L17
- VCCO_15 A17
- VCCO_15 C13
- VCCO_15 D16
- VCCO_15 G15
- VCCO_15 H18
- VCCO_15 K14
- VCCO_34 K4
- VCCO_34 N3
- VCCO_34 P6
- VCCO_34 T2
- VCCO_34 U5
- VCCO_34 V8
- VCCO_35 A7
- VCCO_35 C3
- VCCO_35 D6
- VCCO_35 F2
- VCCO_35 G5
- VCCO_35 J1
- VCCO_0 R9
- VCCO_16 B10
- VCCBRAM F10
- VCCBRAM G11
- VCCAUX F12
- VCCAUX H12
- VCCAUX K12
- VCCAUX M12
- VCCINT F8
- VCCINT G9
- VCCINT G7
- VCCINT H8
- VCCINT J11
- VCCINT J7
- VCCINT K8
- VCCINT L11
- VCCINT L7
- VCCINT M10
- VCCINT M8
- VCCINT N11
- VCCINT N9
- VCCINT N7
- VCCBATT_0 E8

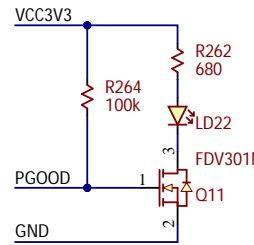
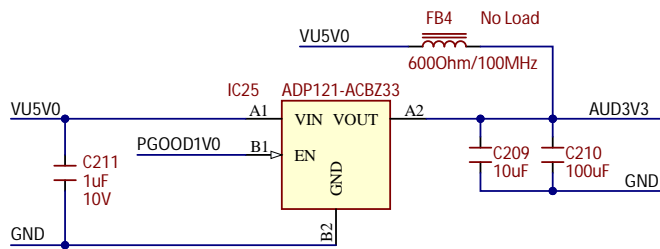
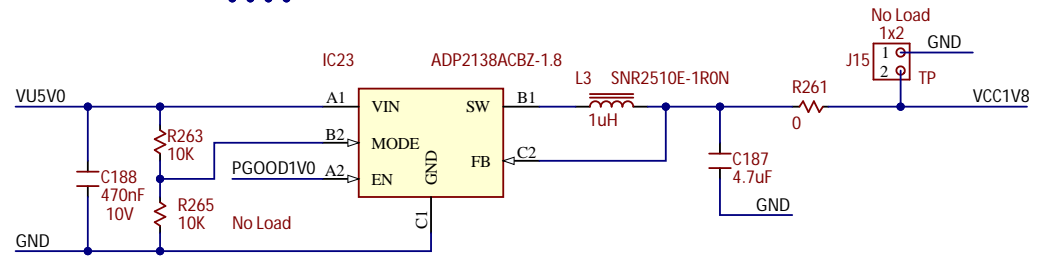
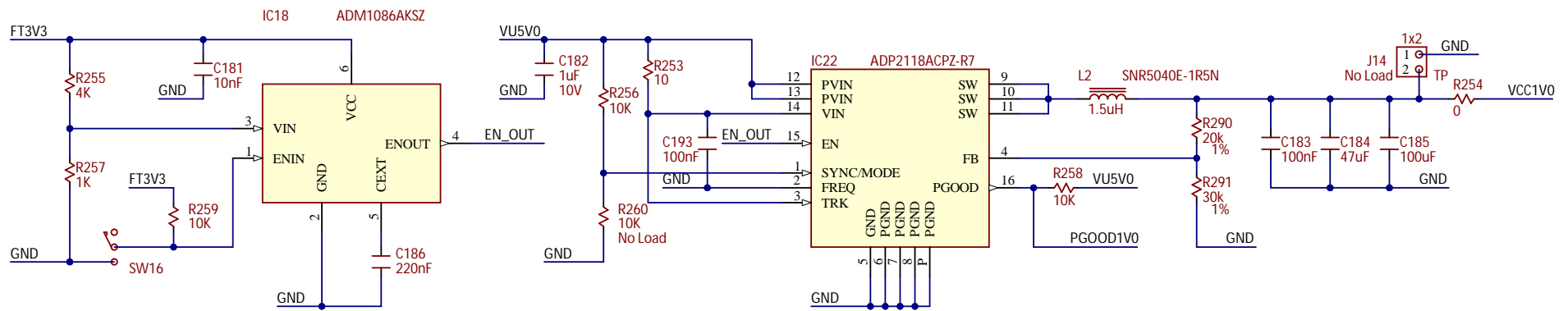
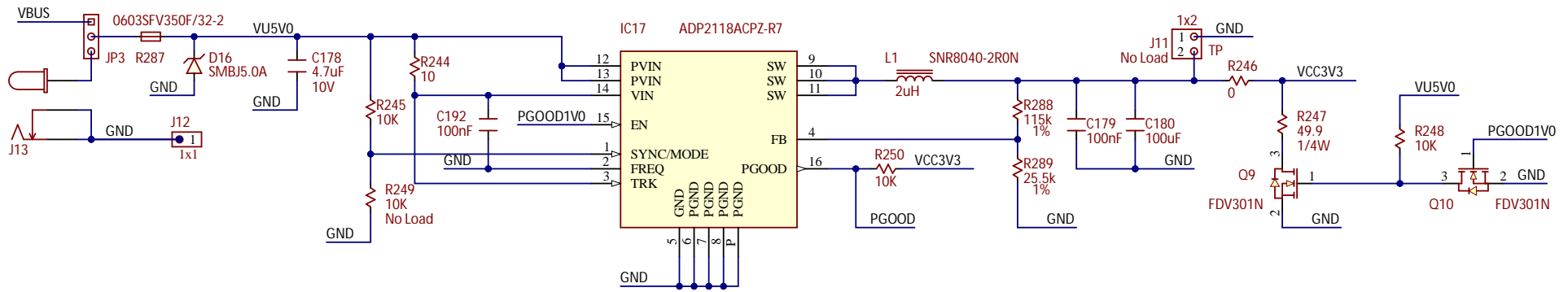
XC7A100T-1CSG324C



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FPGA POWER		
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For more information on the parts used in this design, please refer to:

- <http://www.analog.com/adp2118> (3 A, 1.2 MHz/600 kHz High Efficiency Synchronous Step-Down DC-to-DC Regulator)
- <http://www.analog.com/adm1086> (Voltage Sequencer with Active High, Push-Pull Enable Output)
- <http://www.analog.com/adp2138> (Compact, 800 mA, 3 MHz, Step-Down DC-to-DC Converter)
- <http://www.analog.com/adp121> (CMOS Linear Regulator, 150 mA, Low Quiescent Current)

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