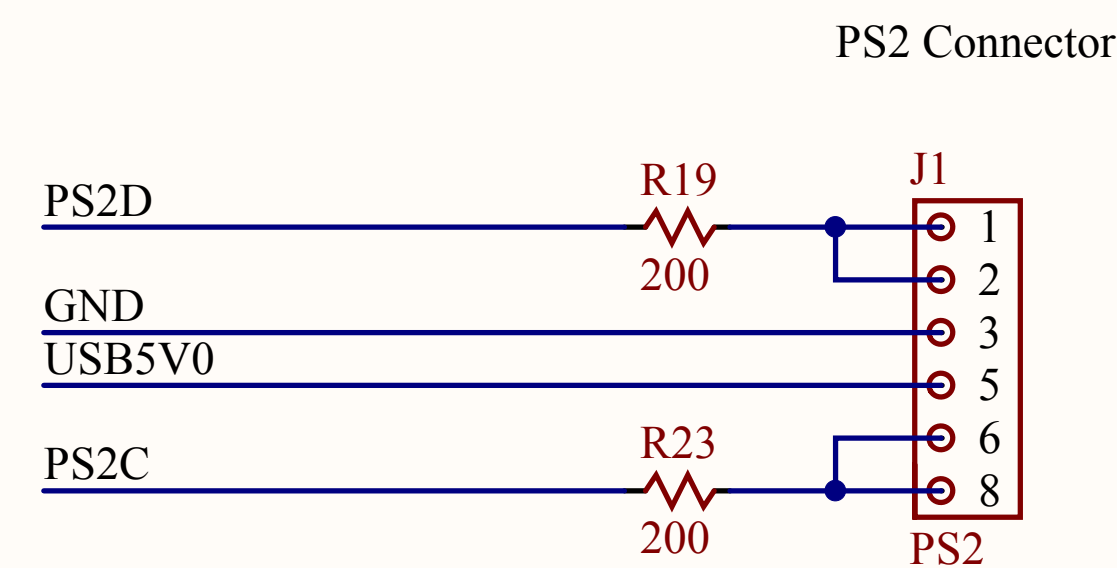
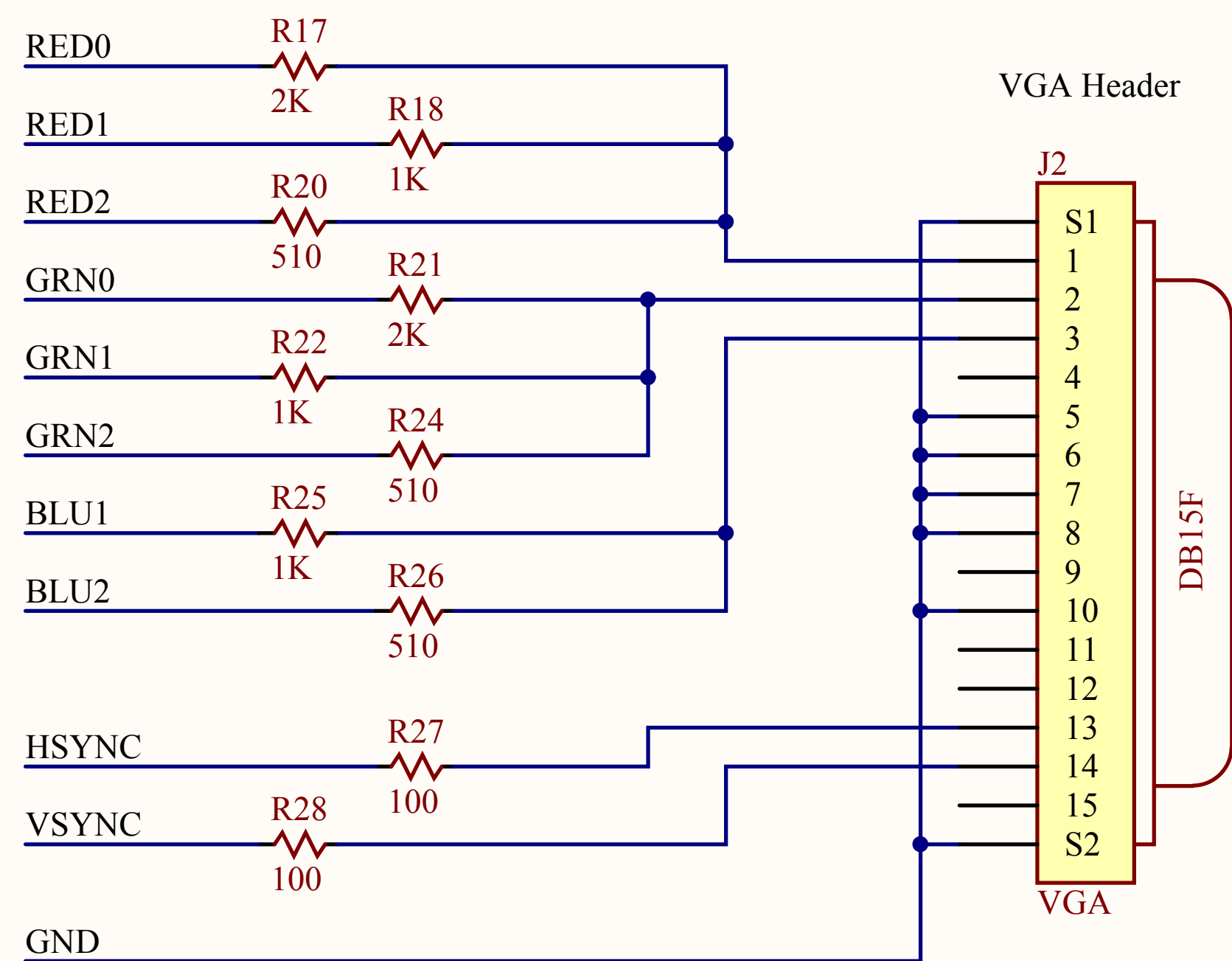
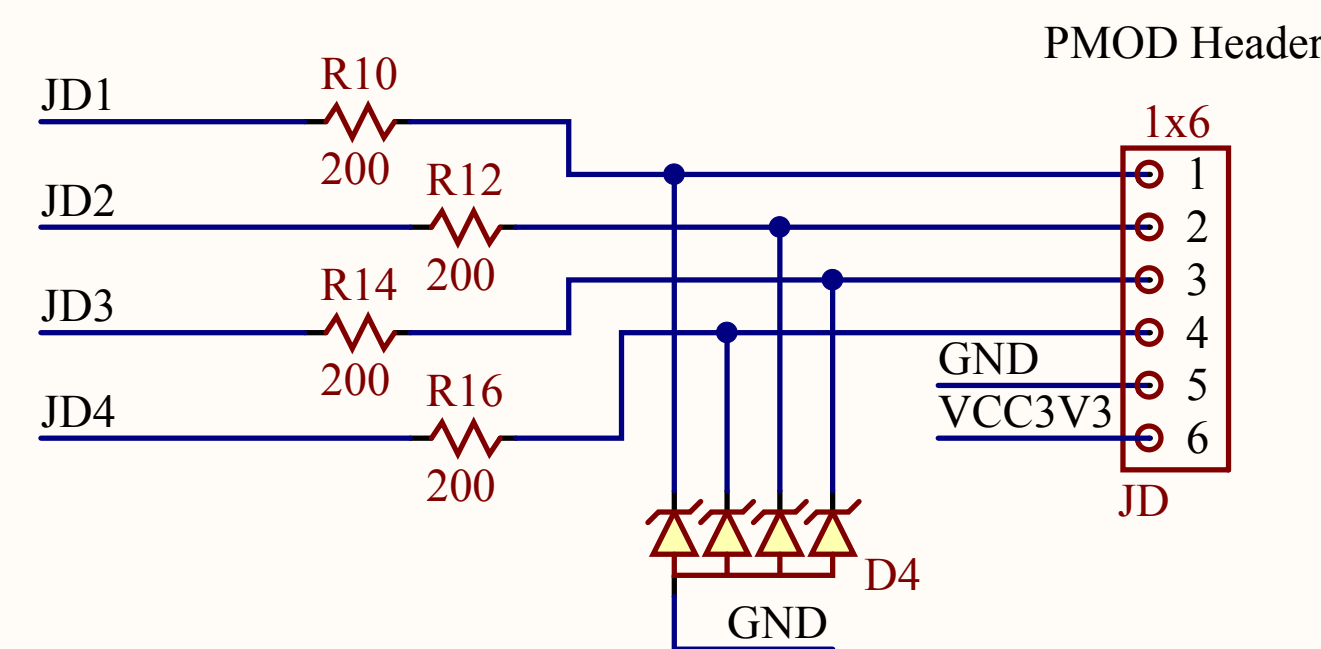
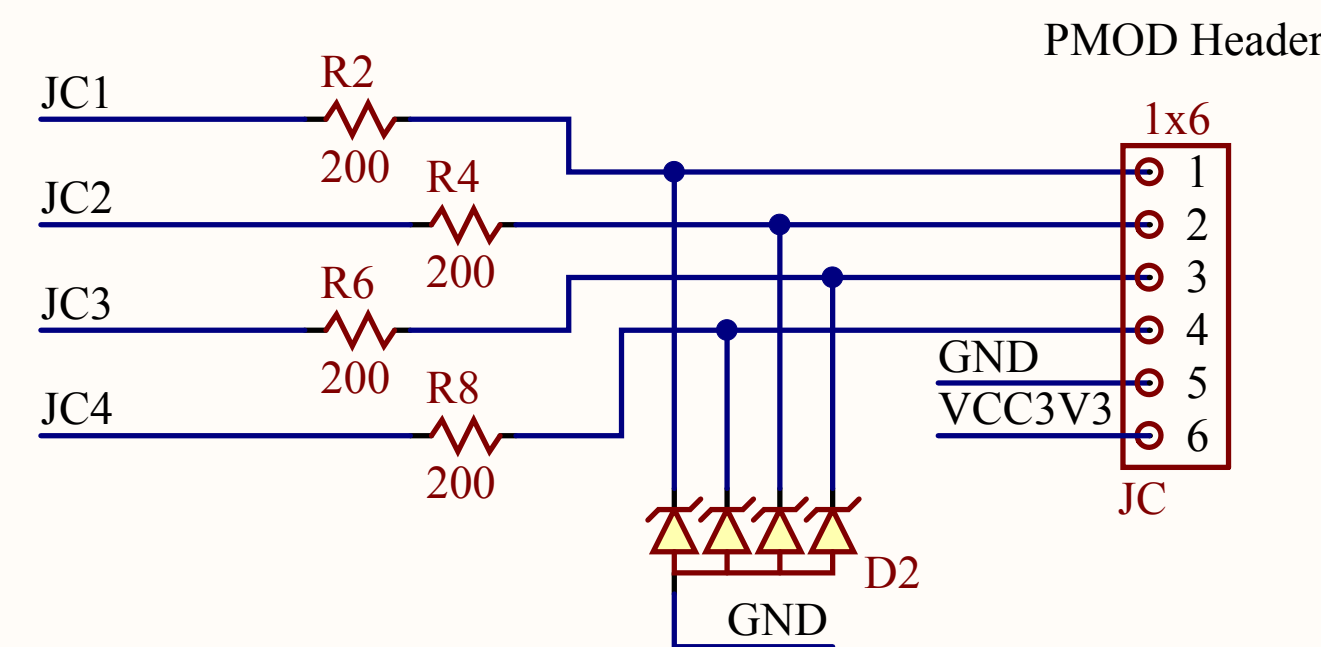
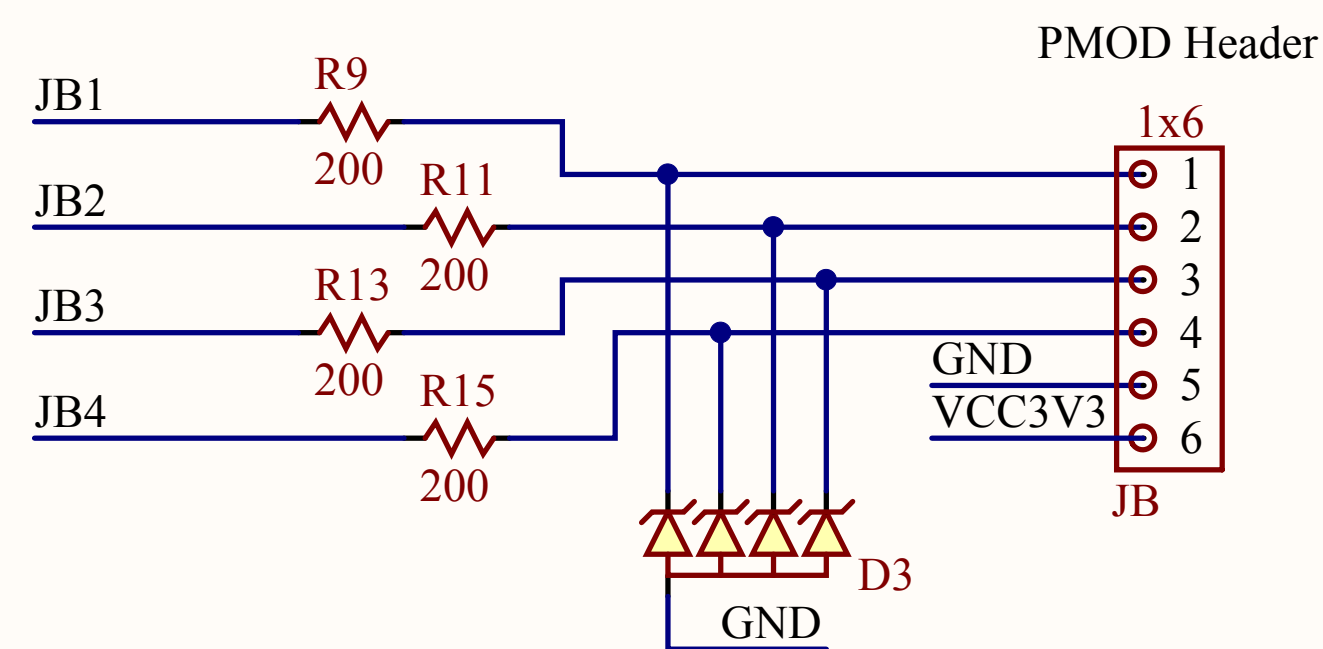
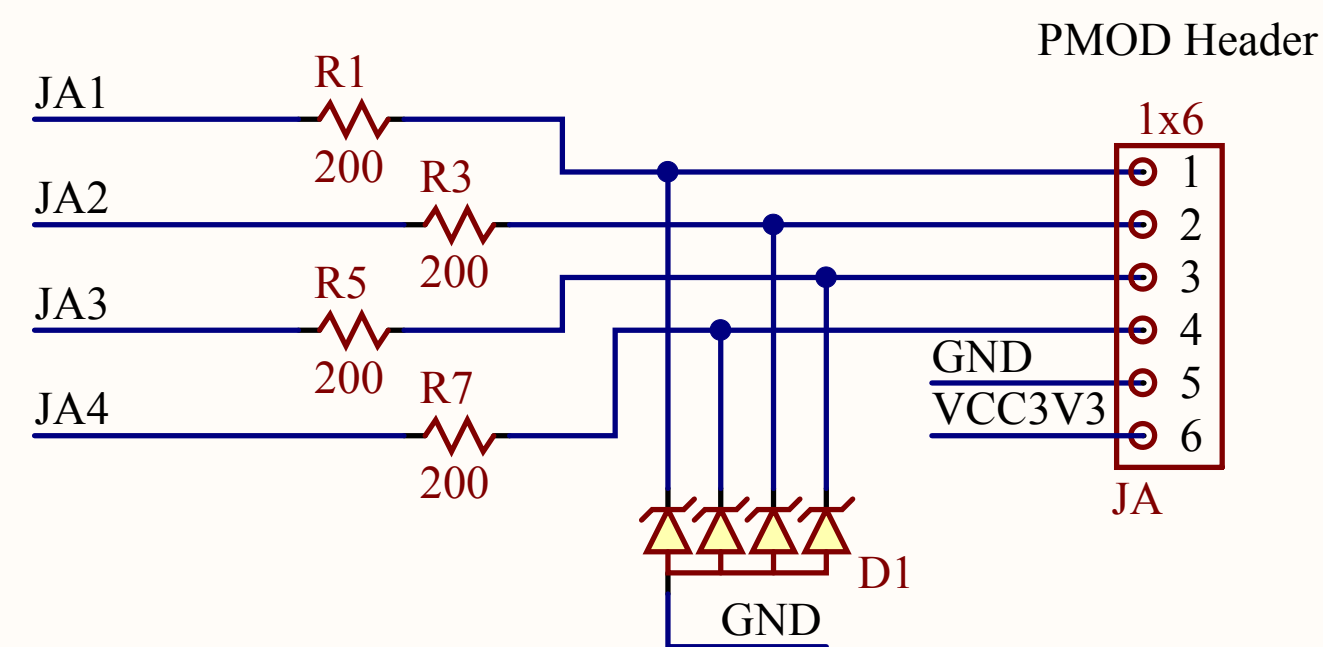




Foot
F1

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F2

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F3

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F4

Title		Rev
Basys 2		D.0
		Copyright
Circuit		
PMOD, VGA & PS2		
Doc#		
500-155		
Engineer		
CC		
Author		
GMA		
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A

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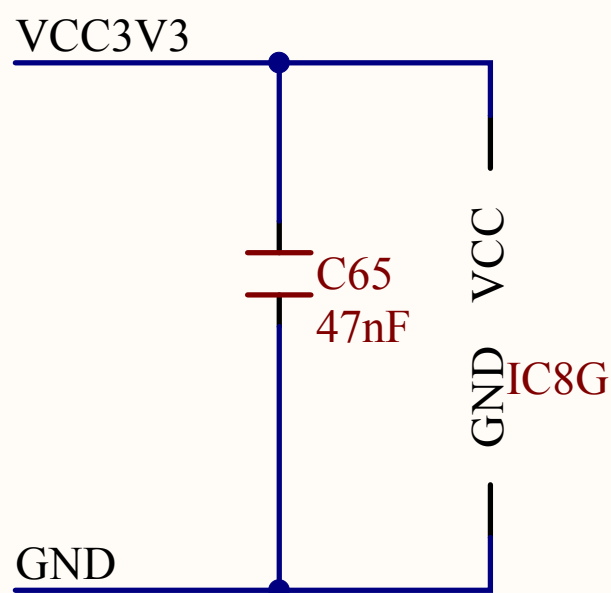
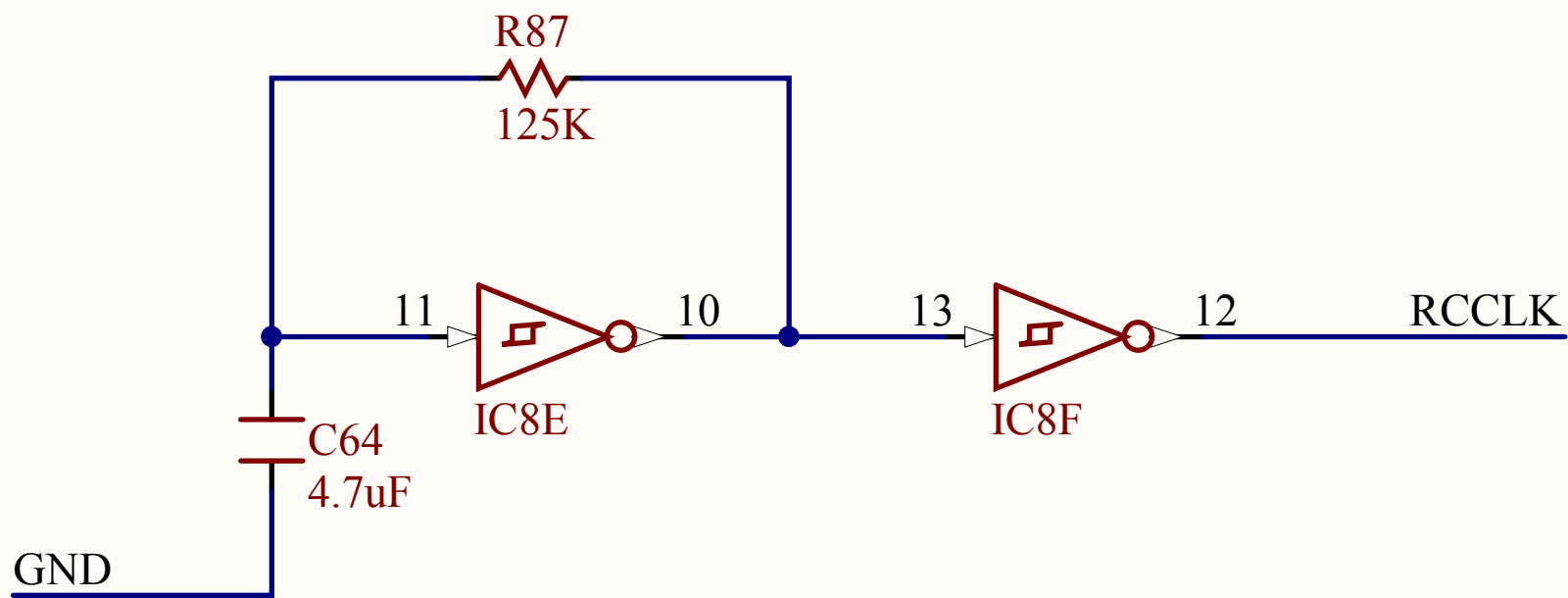
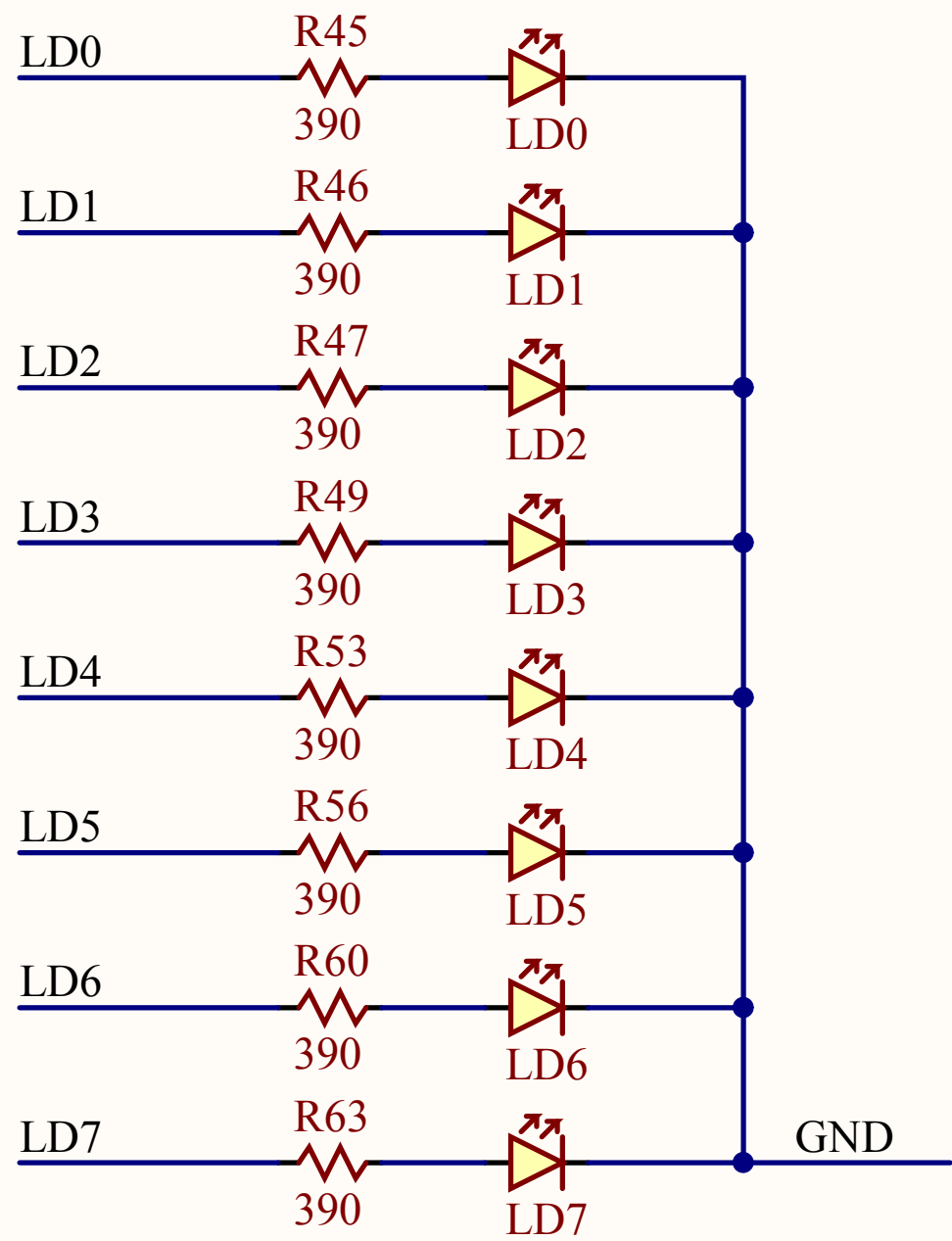
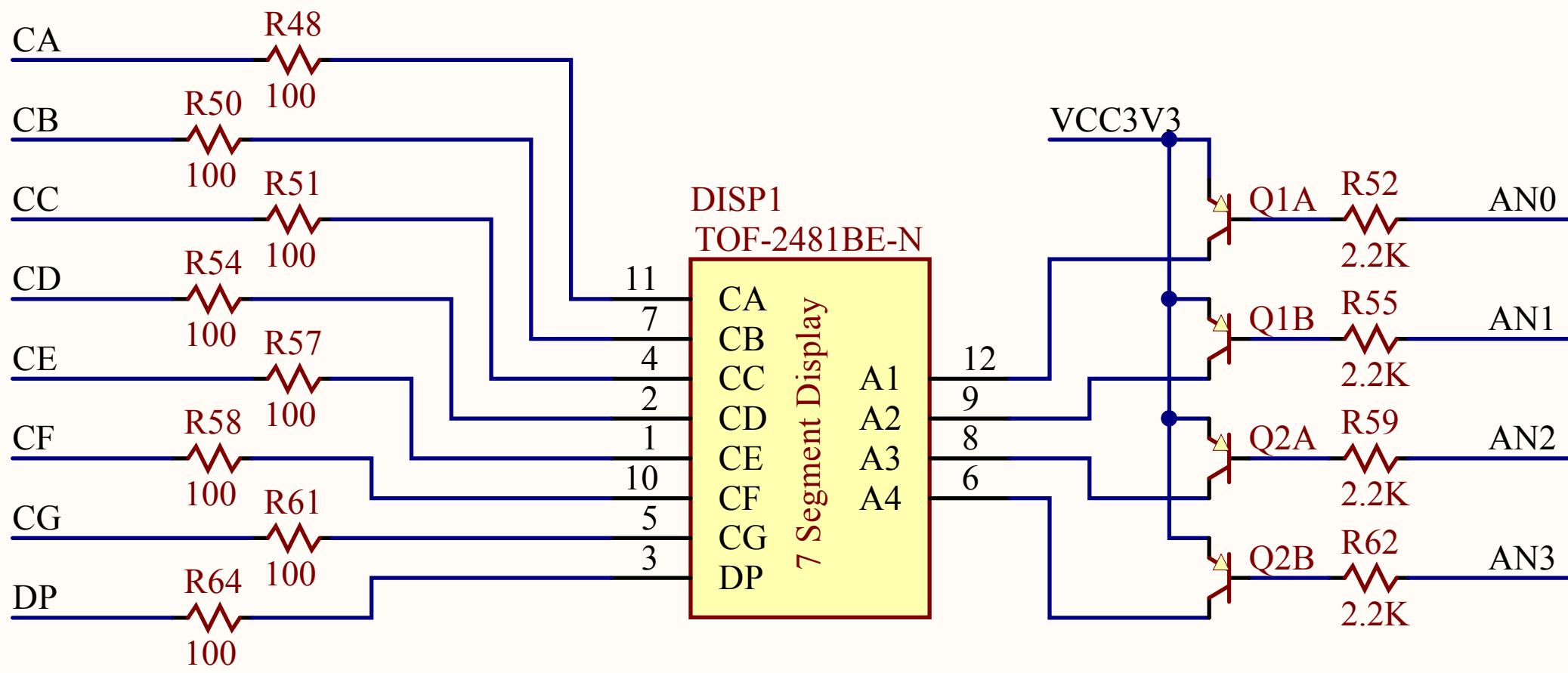
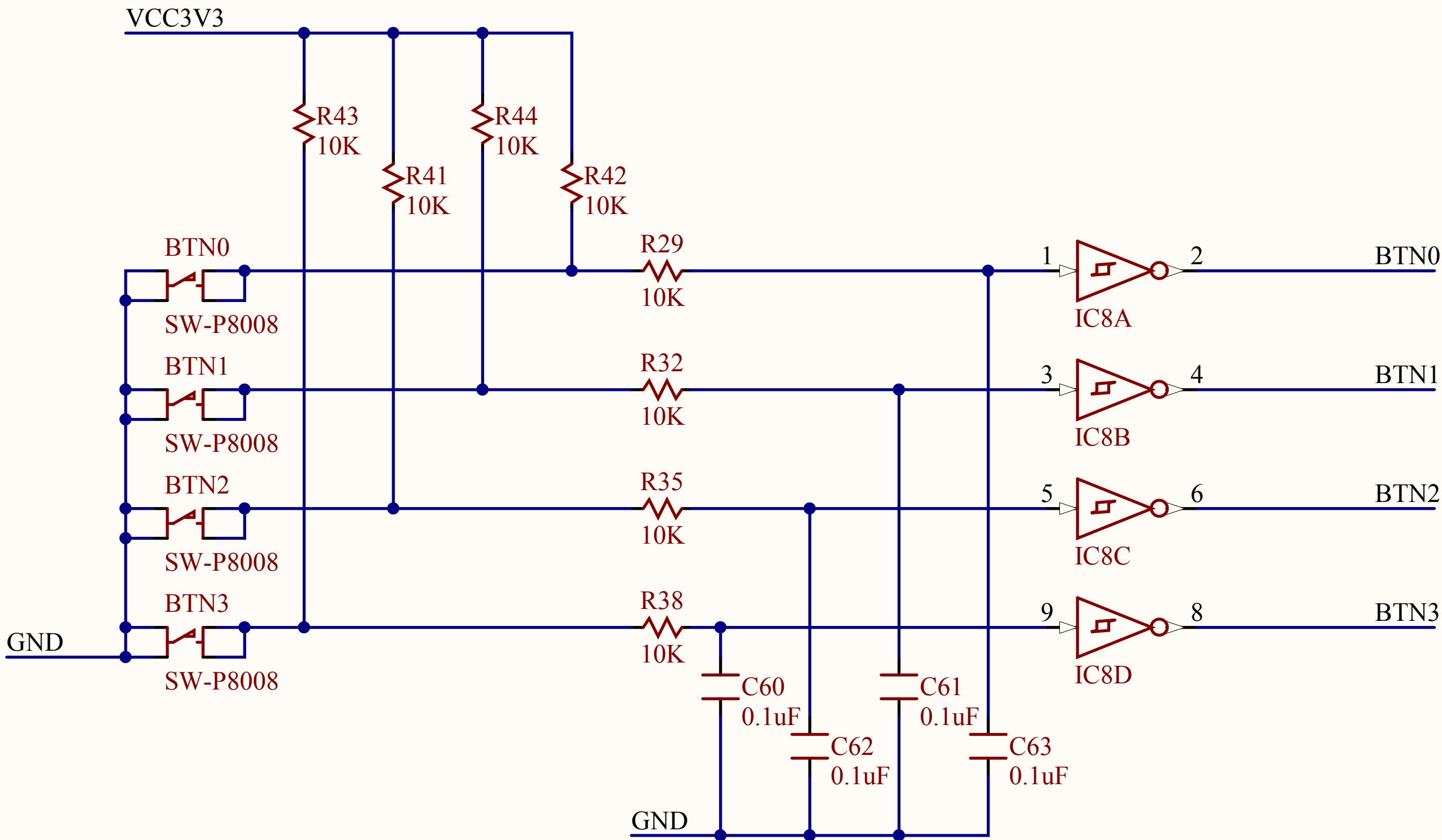
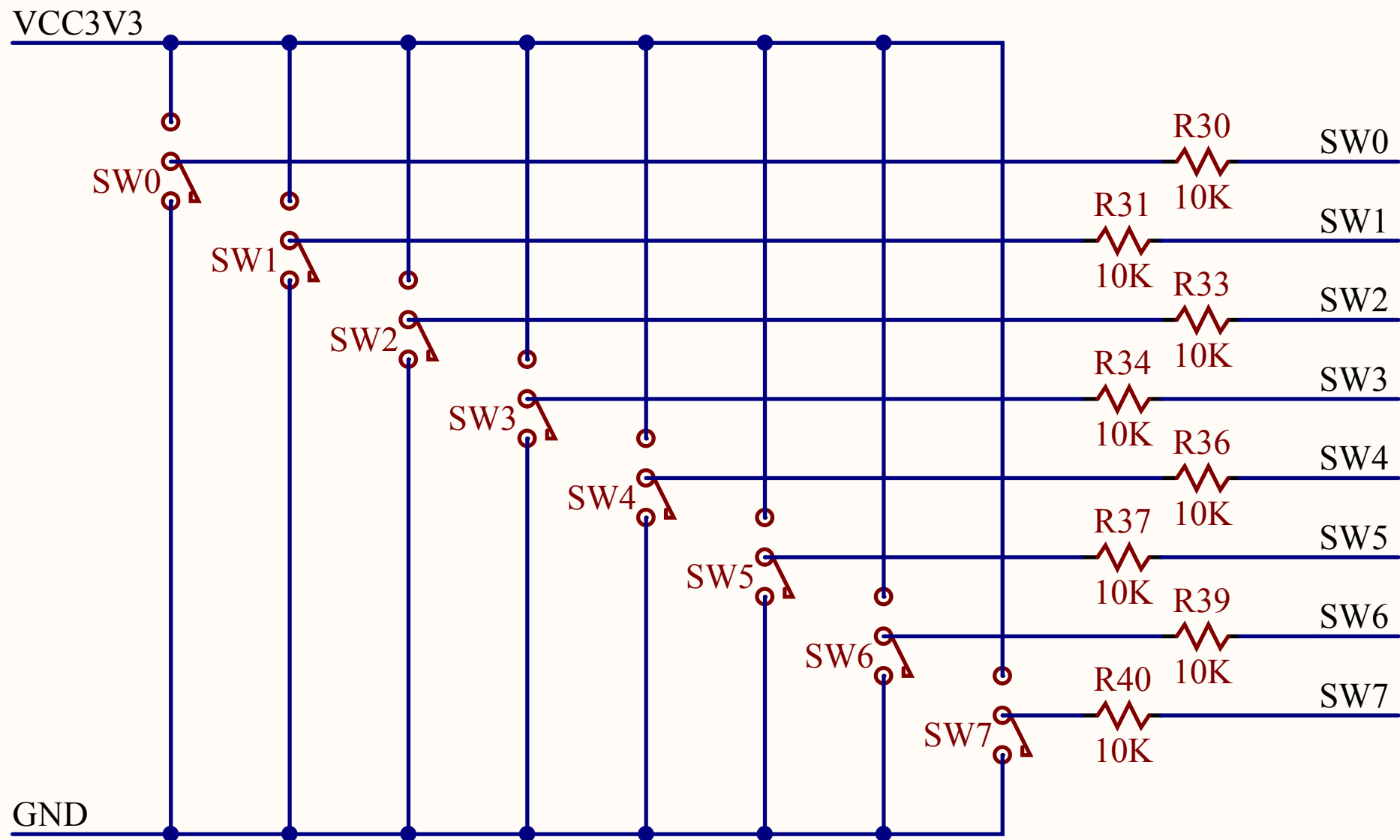
D

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Title		Rev	
Basys 2		D.0	
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General IO			
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A

A

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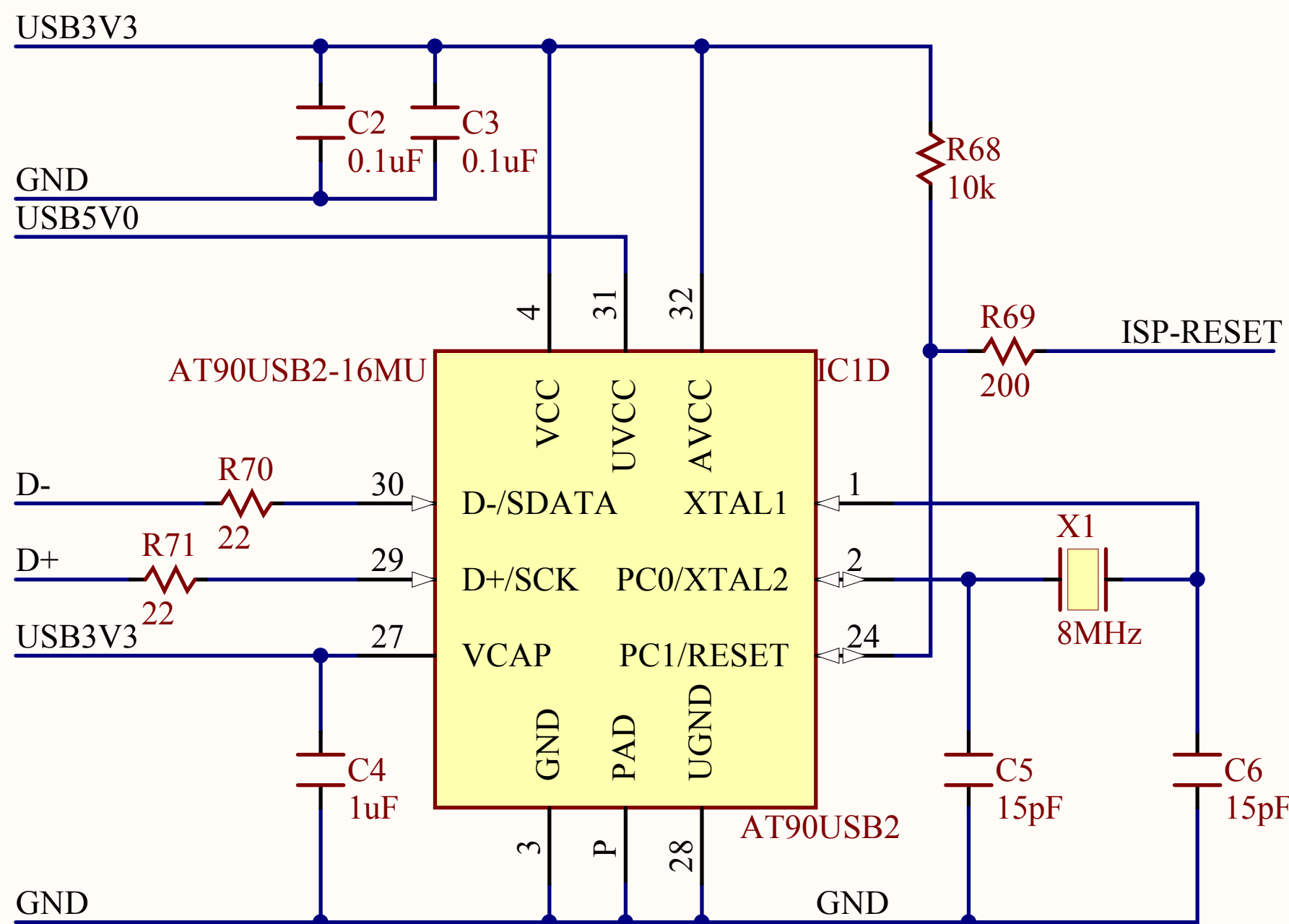
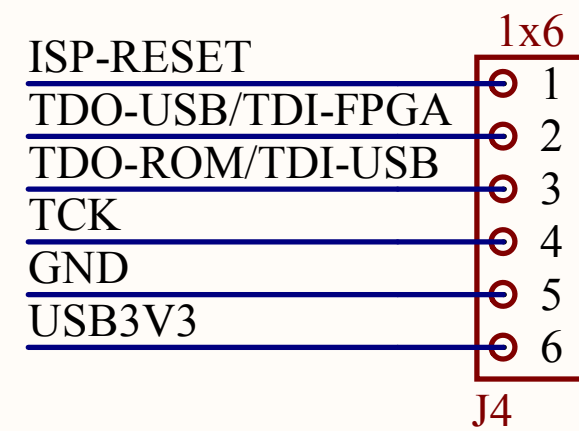
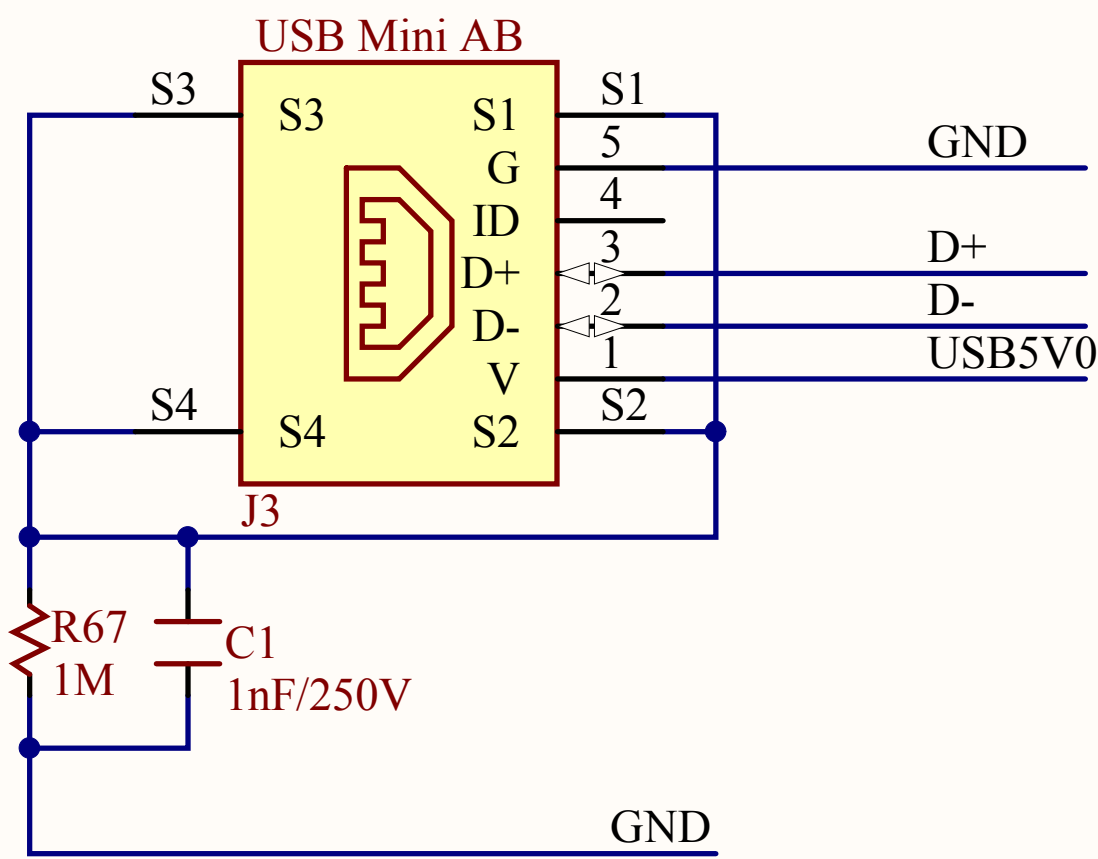
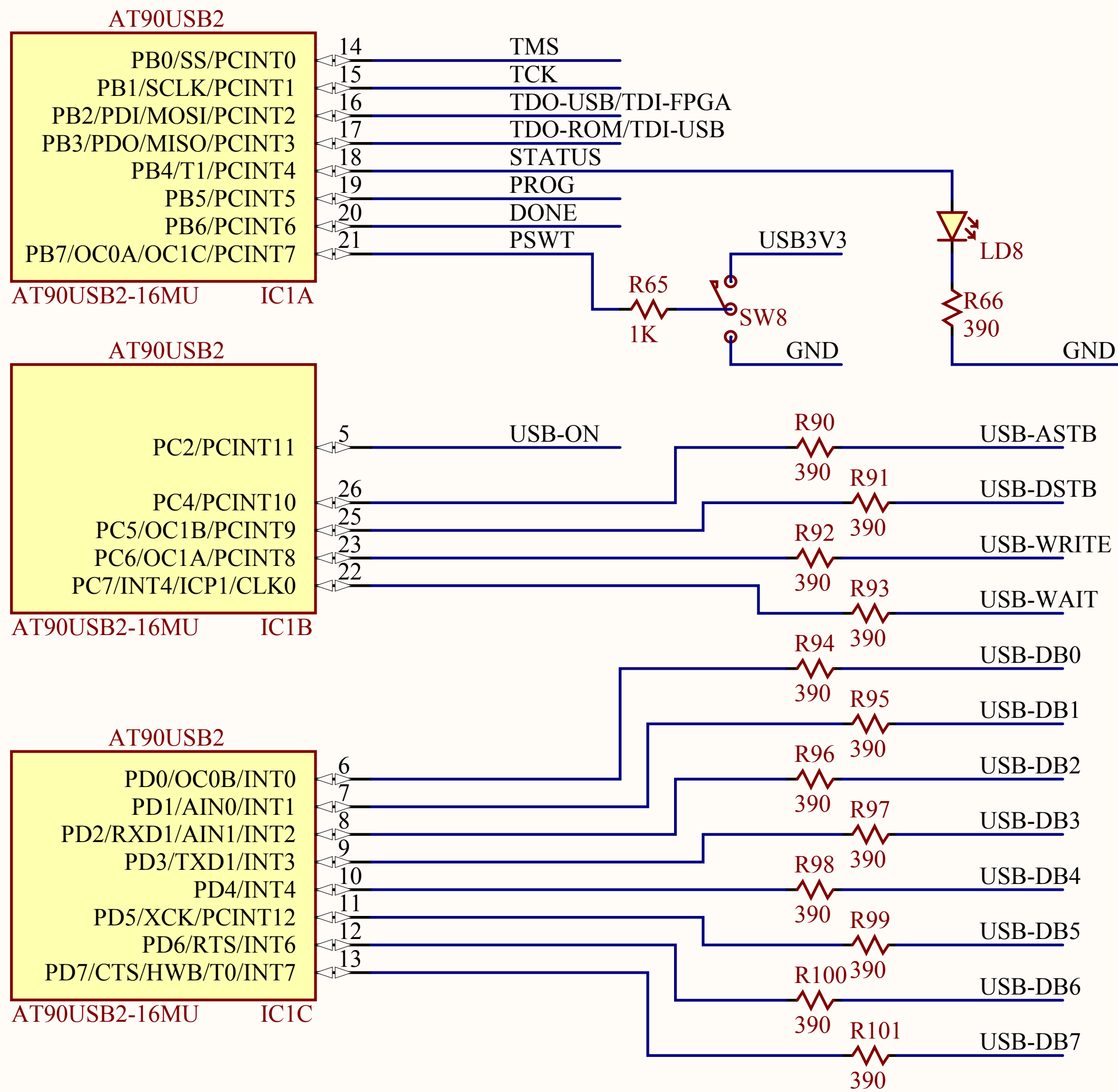
B

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D

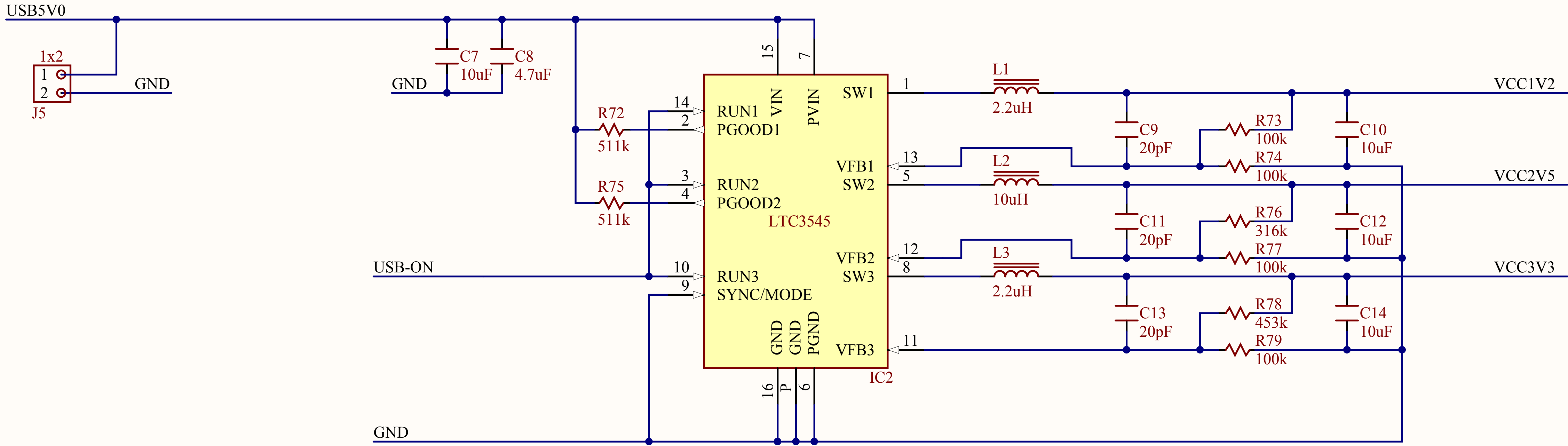


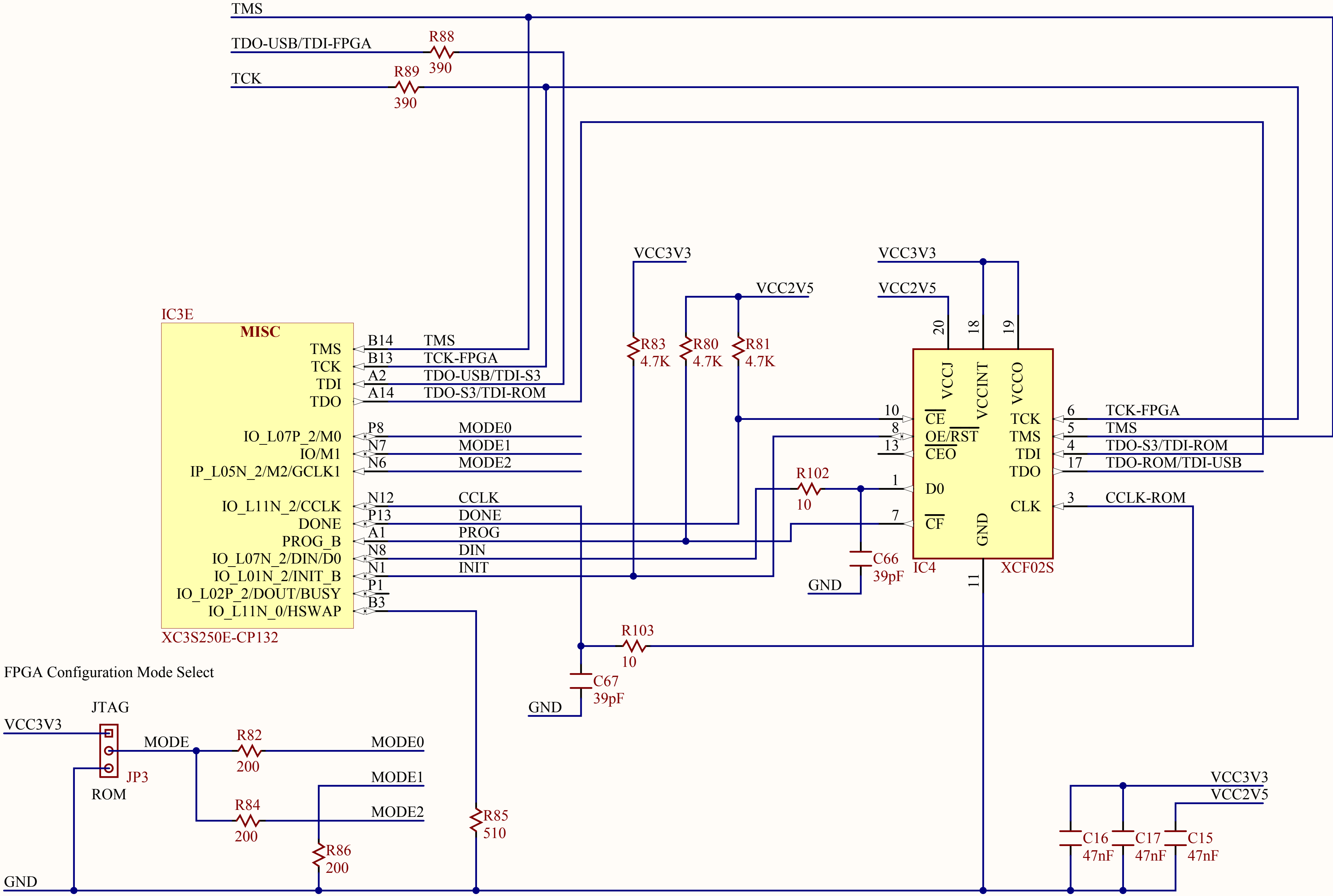
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Basys 2		D.0
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A

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A

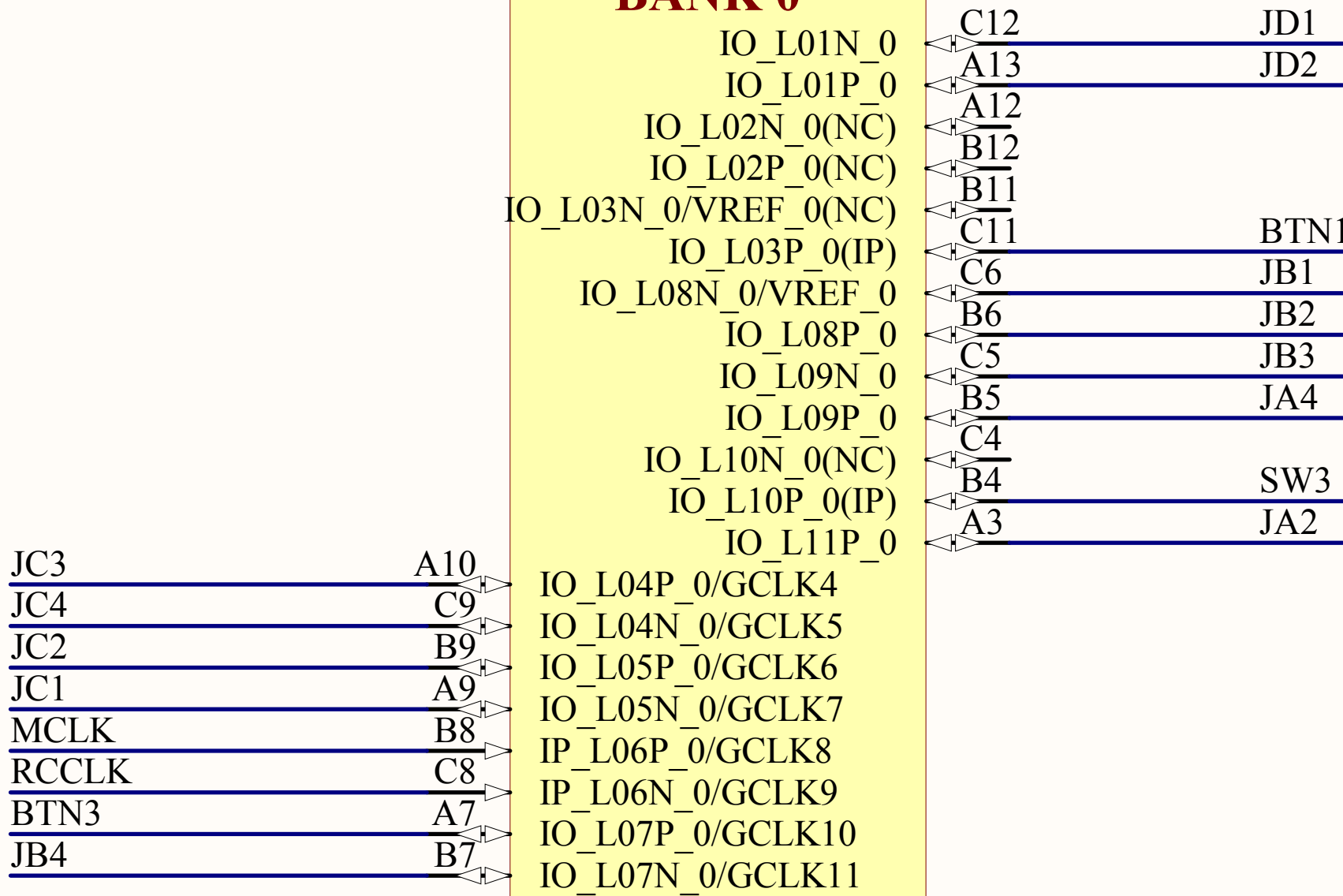
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IC3A

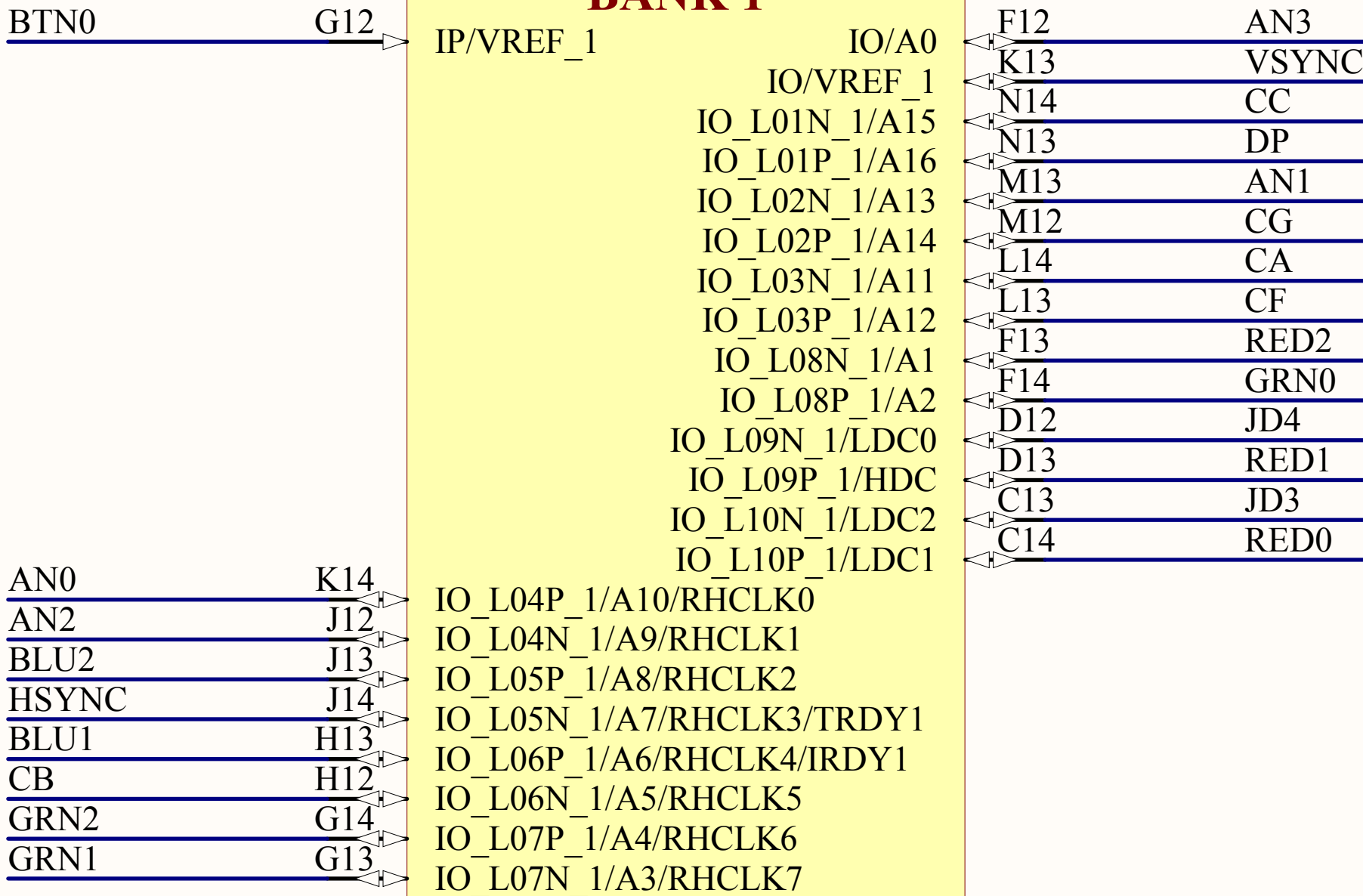
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XC3S100E-CP132

IC3B

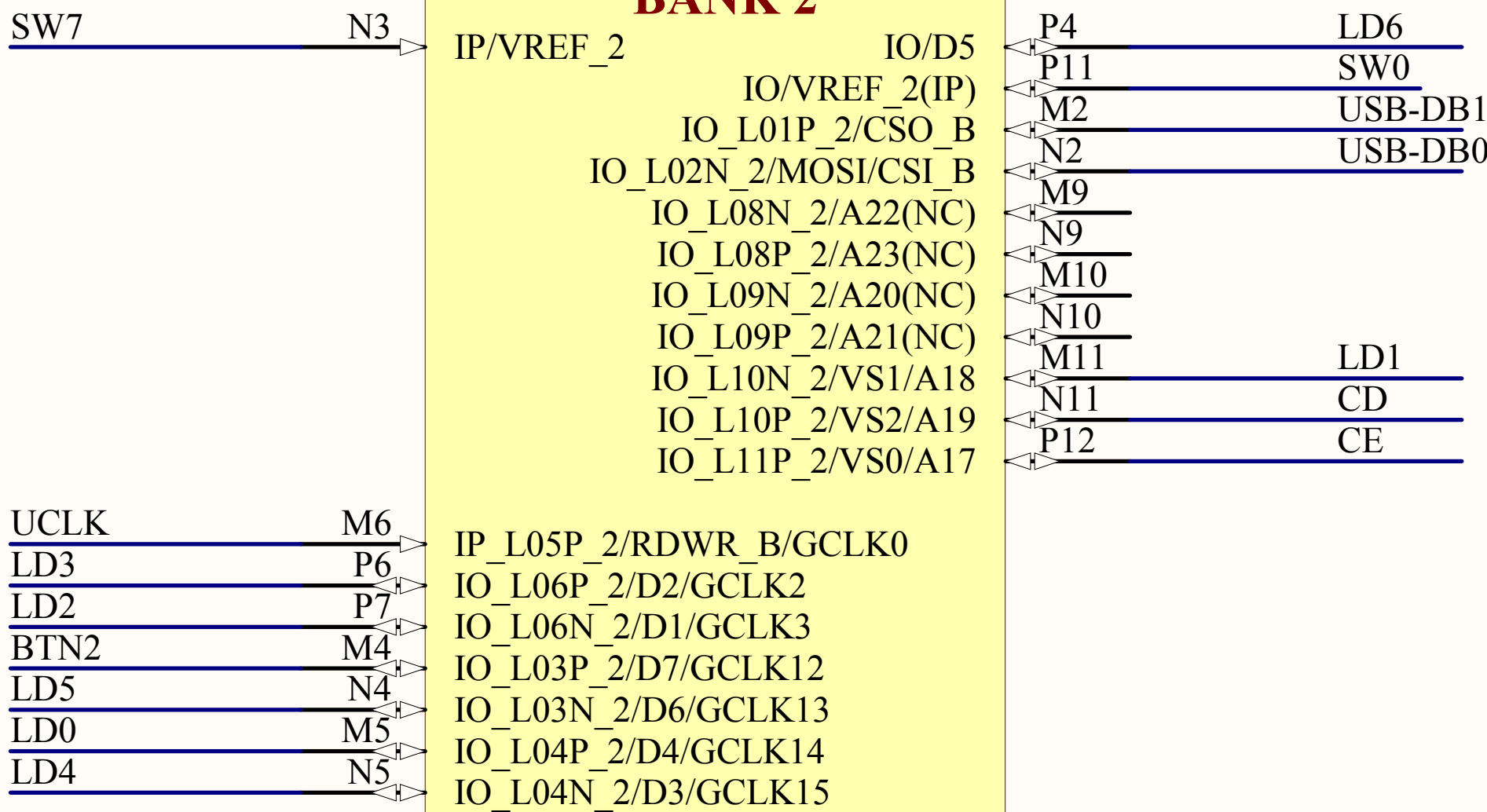
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XC3S250E-CP132

IC3C

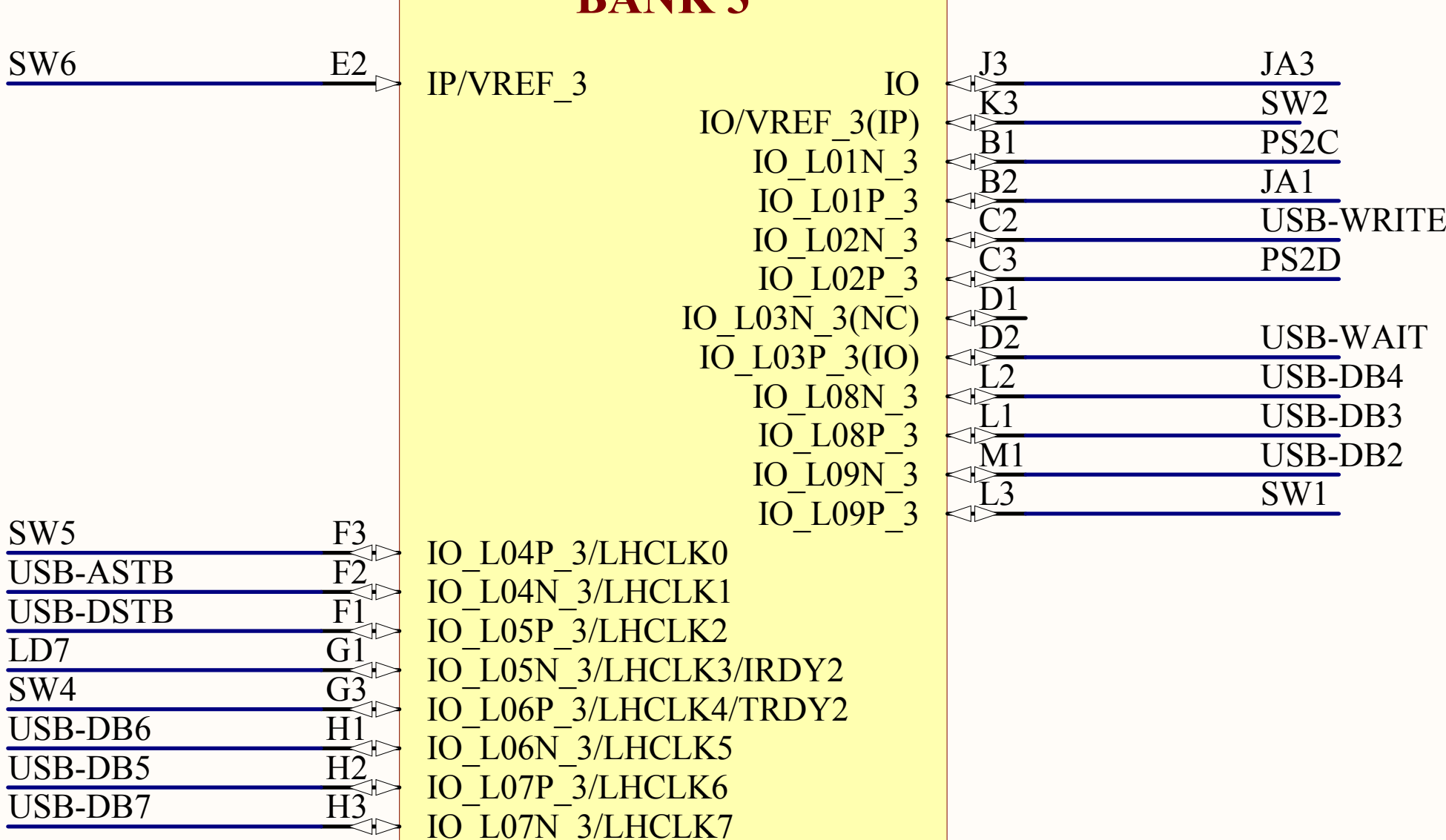
BANK 2



XC3S250E-CP132

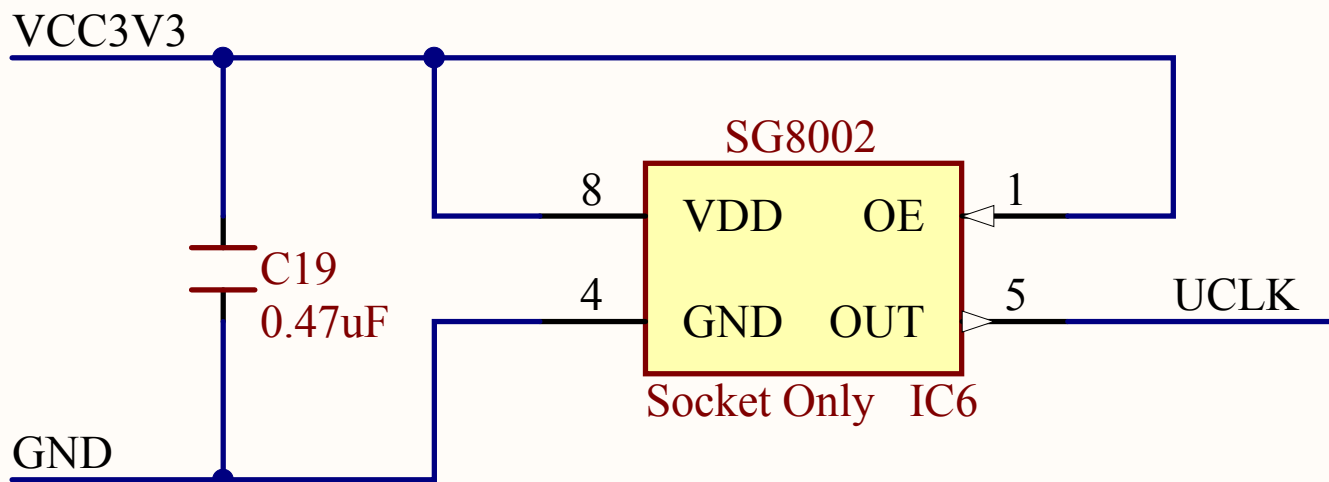
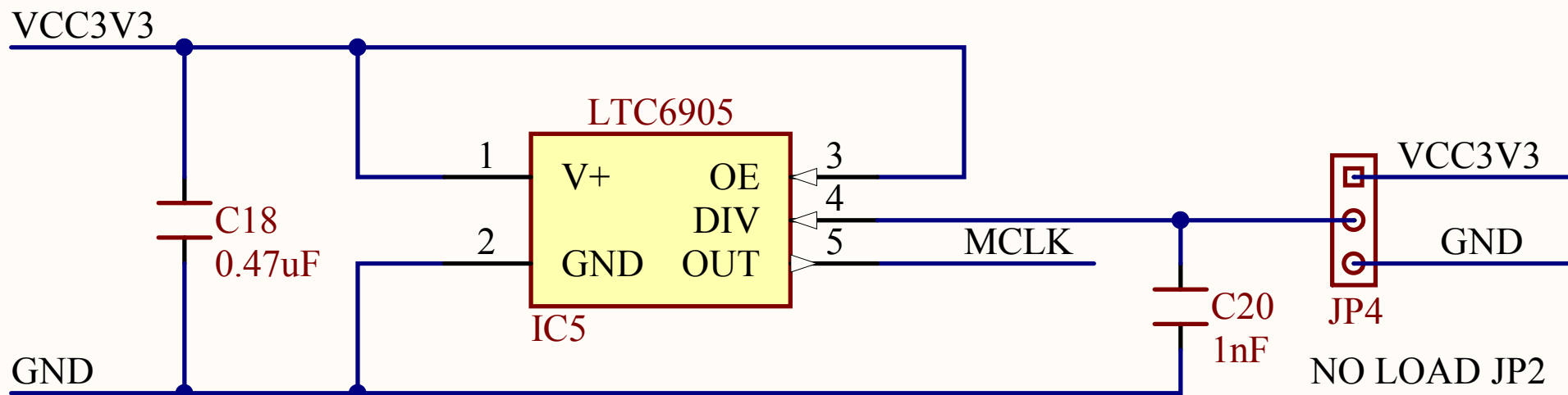
IC3D

BANK 3



XC3S250E-CP132

Note:
Short DIV to 3.3V for 100MHz
No shorting block for 50MHz
Short DIV to GND for 25MHz



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Circuit FPGA and Clocks	 DIGILENT www.digilentinc.com	
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