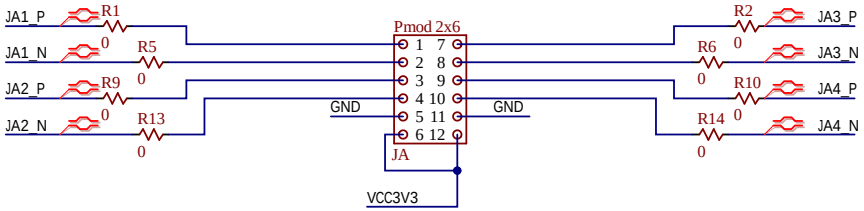

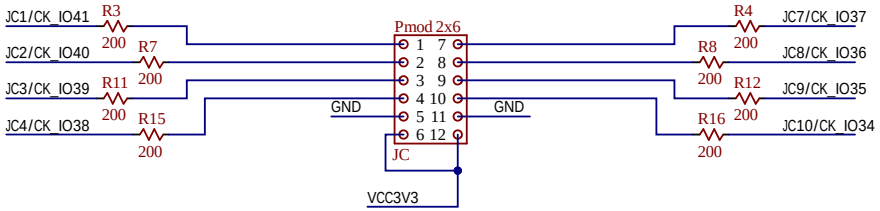

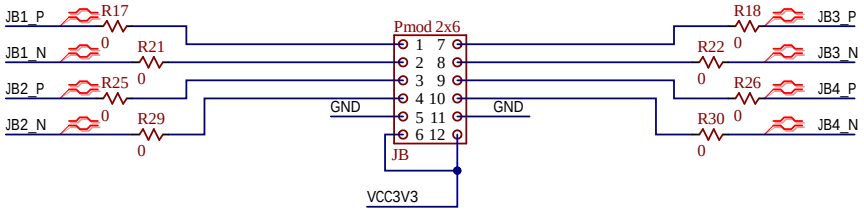

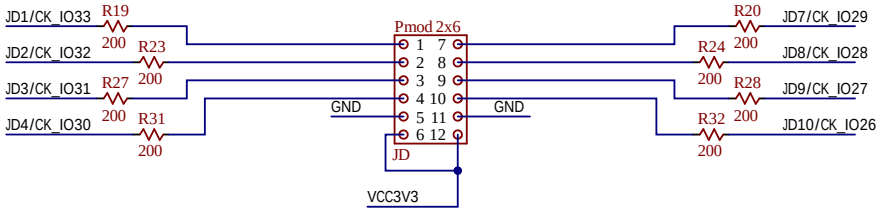

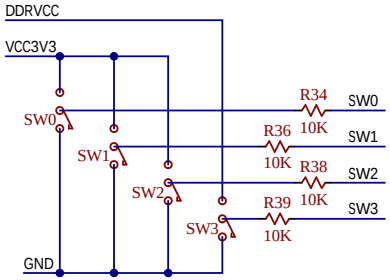

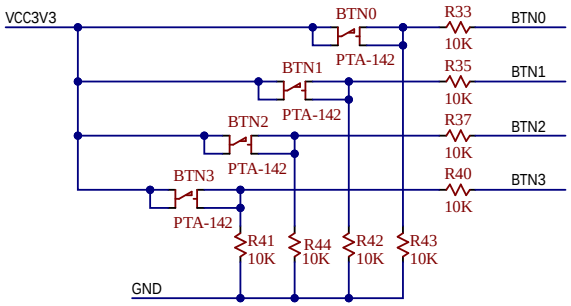

Arty S7

Xilinx | Digilent Inc. | CE | ROHS | Chinese ROHS

Foot F1
Foot F2
Foot F3
Foot F4

Title	Arty S7
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Circuit	PMOD, BTN, SWTs
Doc#	500-352
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Author	GMA
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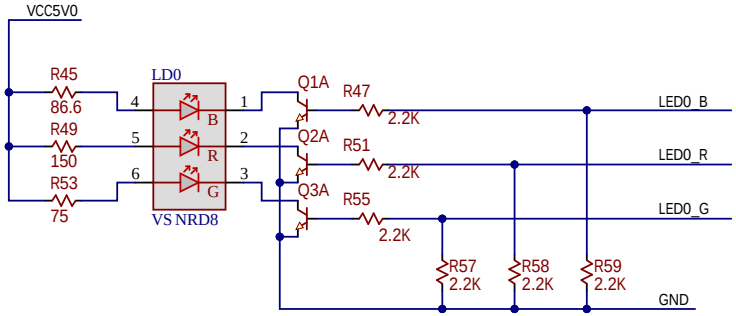

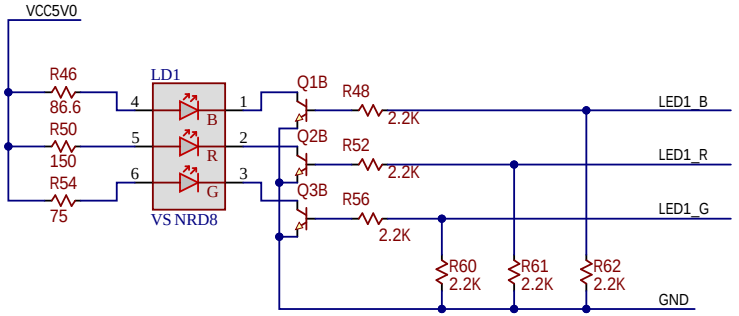

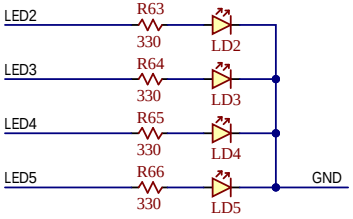

Title	Arty S7
Rev	E.2
Circuit	LEDs
Doc#	500-352
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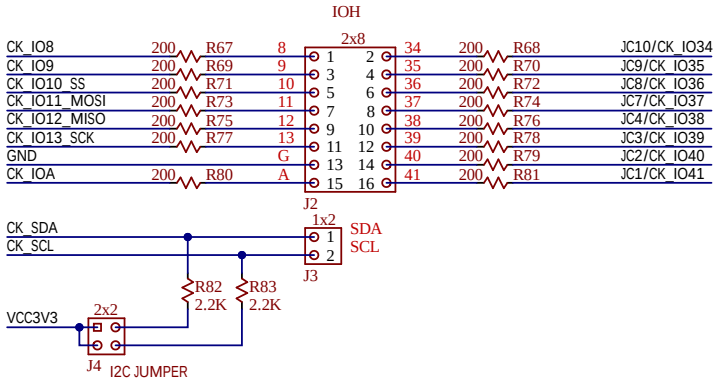
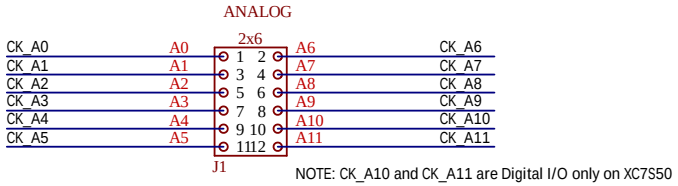
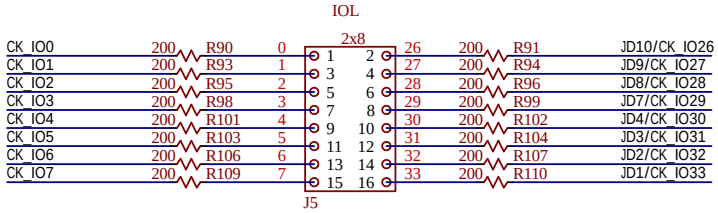
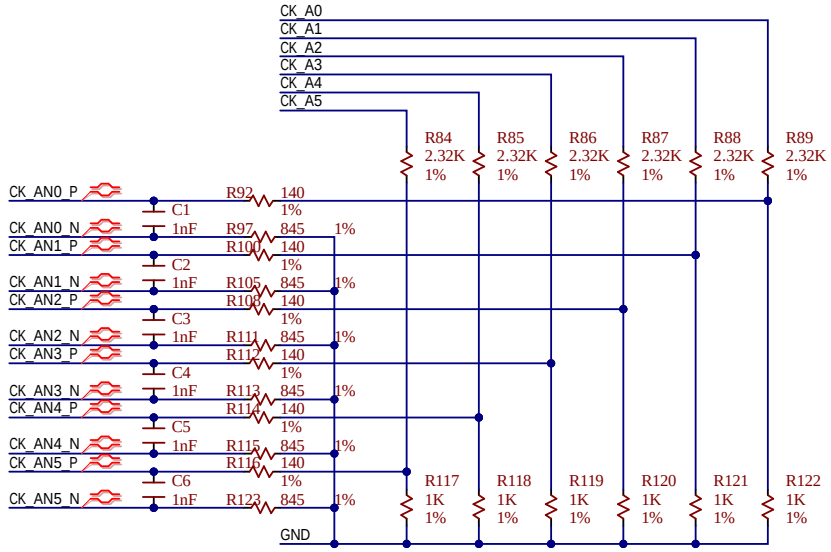
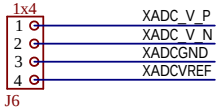


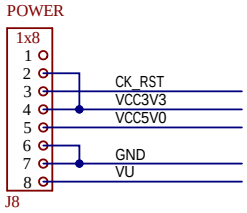


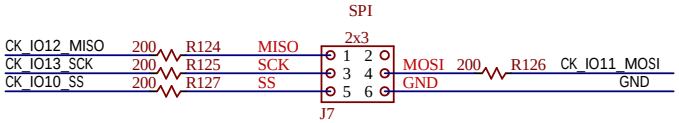




Note: Terminate N signals next to Analog Header







Title	Arty S7
Rev	E.2
Circuit	CHipKIT IO
Doc#	500-352
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Author	GMA
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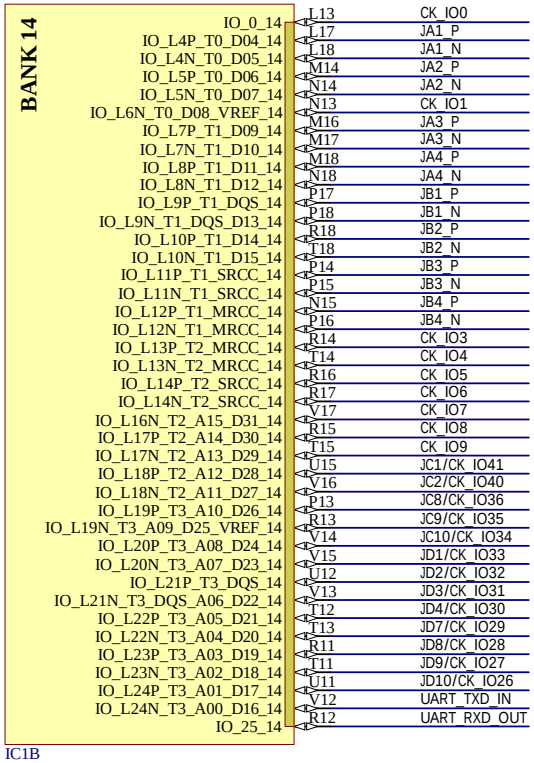
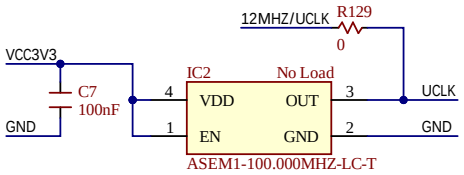
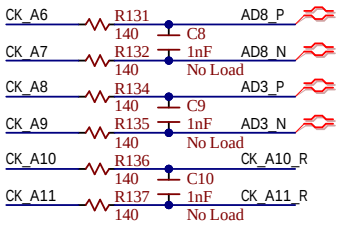
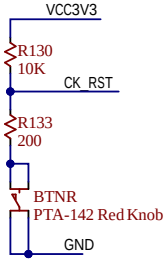
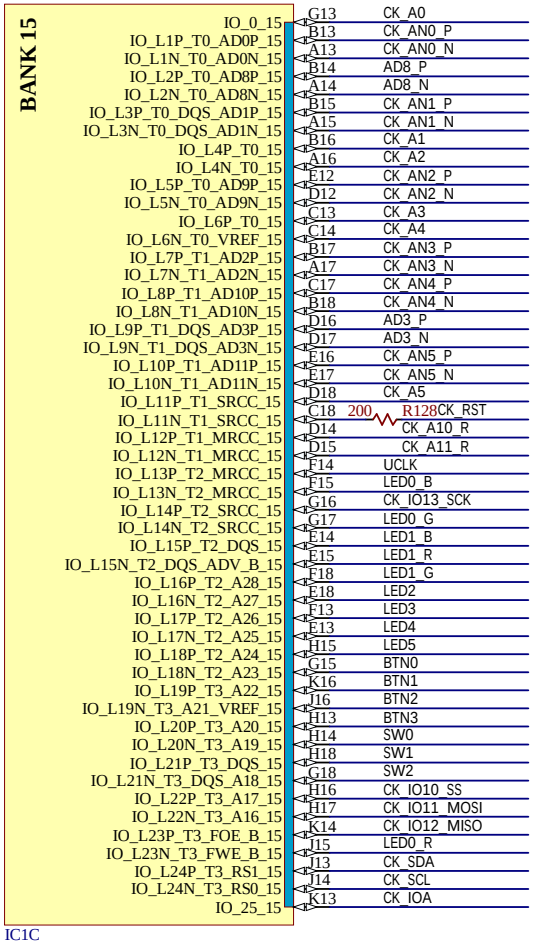


IC1B









IC1C

Net Name	XC7S50 XADC	XC7S25 XADC	PIN NAME
CK_AN0_P	Vaux0_v_p	Vaux0_v_p	B13
CK_AN0_N	Vaux0_v_n	Vaux0_v_n	A13
AD8_P	Vaux8_v_p	Vaux8_v_p	B14
AD8_N	Vaux8_v_n	Vaux8_v_n	A14
CK_AN1_P	Vaux1_v_p	Vaux1_v_p	B15
CK_AN1_N	Vaux1_v_n	Vaux1_v_n	A15
CK_AN2_P	Vaux9_v_p	Vaux2_v_p	E12
CK_AN2_N	Vaux9_v_n	Vaux2_v_n	D12
CK_AN3_P	Vaux2_v_p	Vaux10_v_p	B17
CK_AN3_N	Vaux2_v_n	Vaux10_v_n	A17
CK_AN4_P	Vaux10_v_p	Vaux3_v_p	C17
CK_AN4_N	Vaux10_v_n	Vaux3_v_n	B18
AD3_P	Vaux3_v_p	Vaux11_v_p	D16
AD3_N	Vaux3_v_n	Vaux11_v_n	D17
CK_AN5_P	Vaux11_v_p	Vaux4_v_p	E16
CK_AN5_N	Vaux11_v_n	Vaux4_v_n	E17
CK_A10_R	NA	Vaux5_v_p	D14
CK_A11_R	NA	Vaux5_v_n	D15

Title: Arty S7

Rev: E.2

Circuit: FPGA Banks

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Engineer MTA

Author GMA

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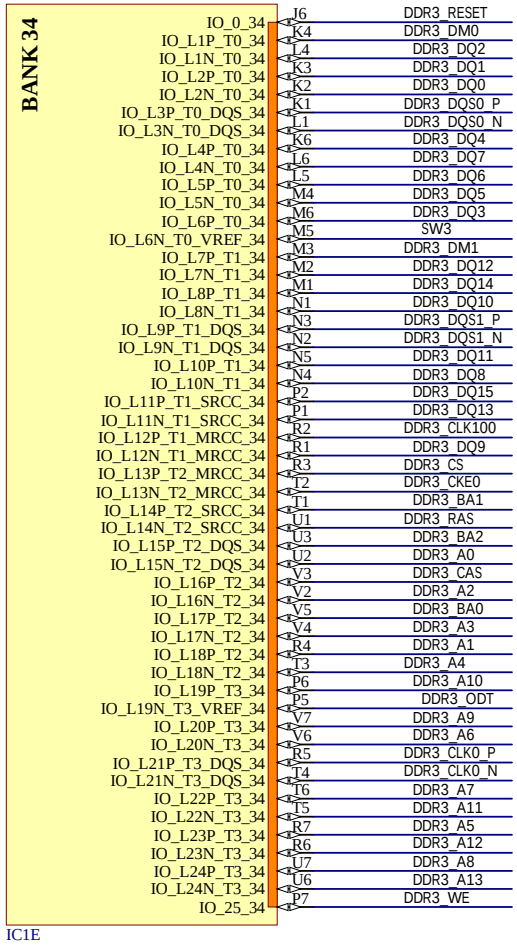

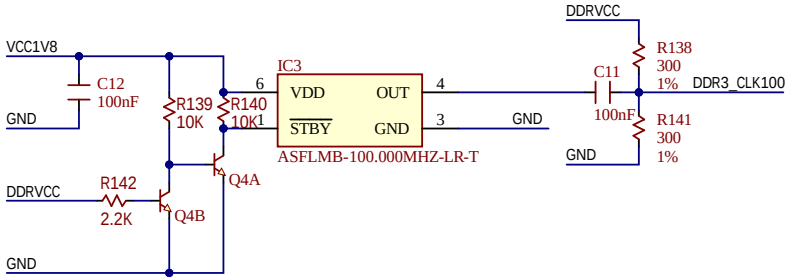

Title	Arty S7
Rev	E.2
Circuit	FPGA Banks
Doc#	500-352
Engineer	MTA
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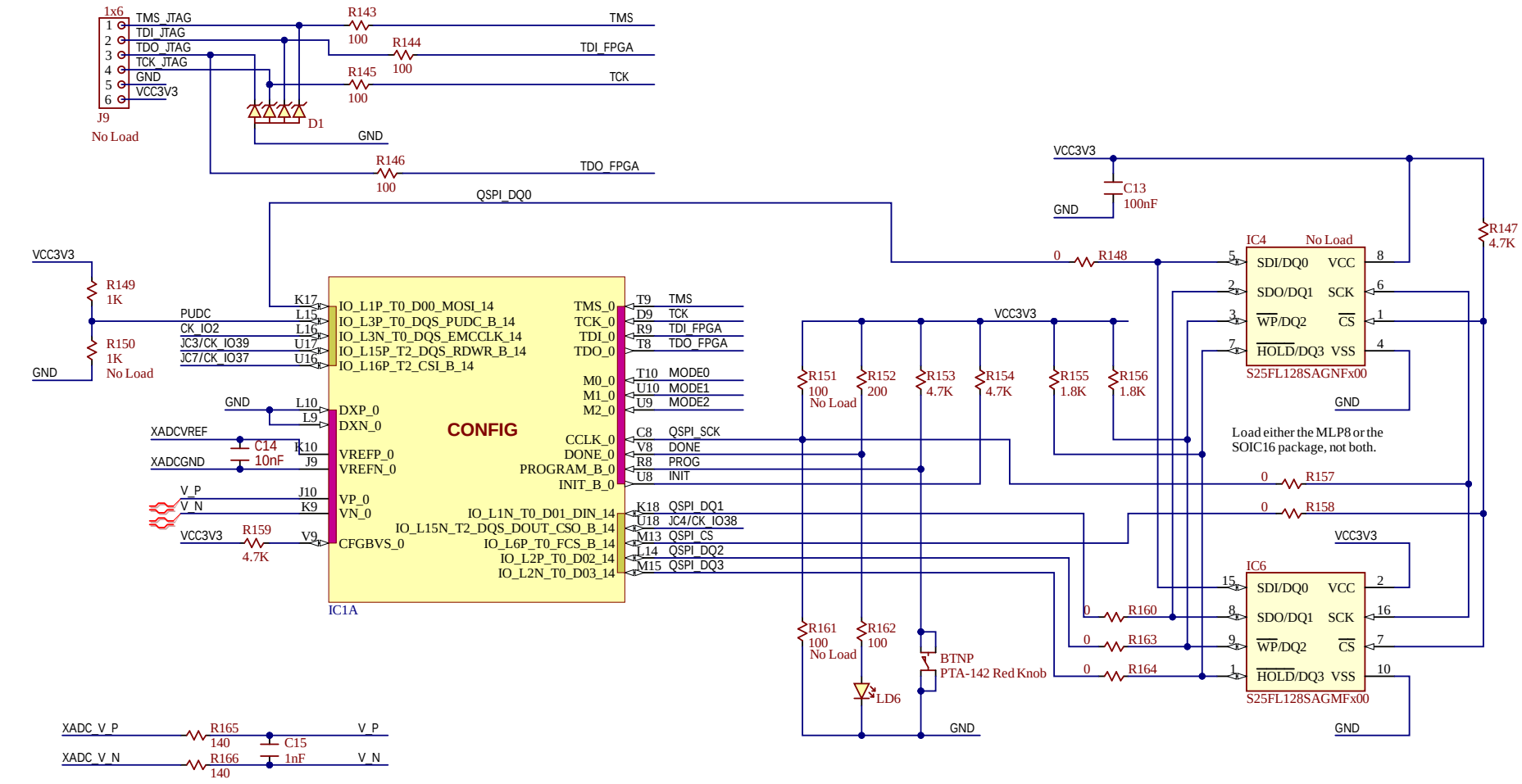

Due to supply chain constraints, S25FL127SABMFx00x or S25FL128SAGMFx00x may be loaded for IC6. Please see the Arty S7 Reference Manual for information about the differences between these Quad-SPI Flash Memories and how to identify which memory is installed on your board.

Title	Arty S7
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Circuit	CONFIG, SPI FLASH
Doc#	500-352
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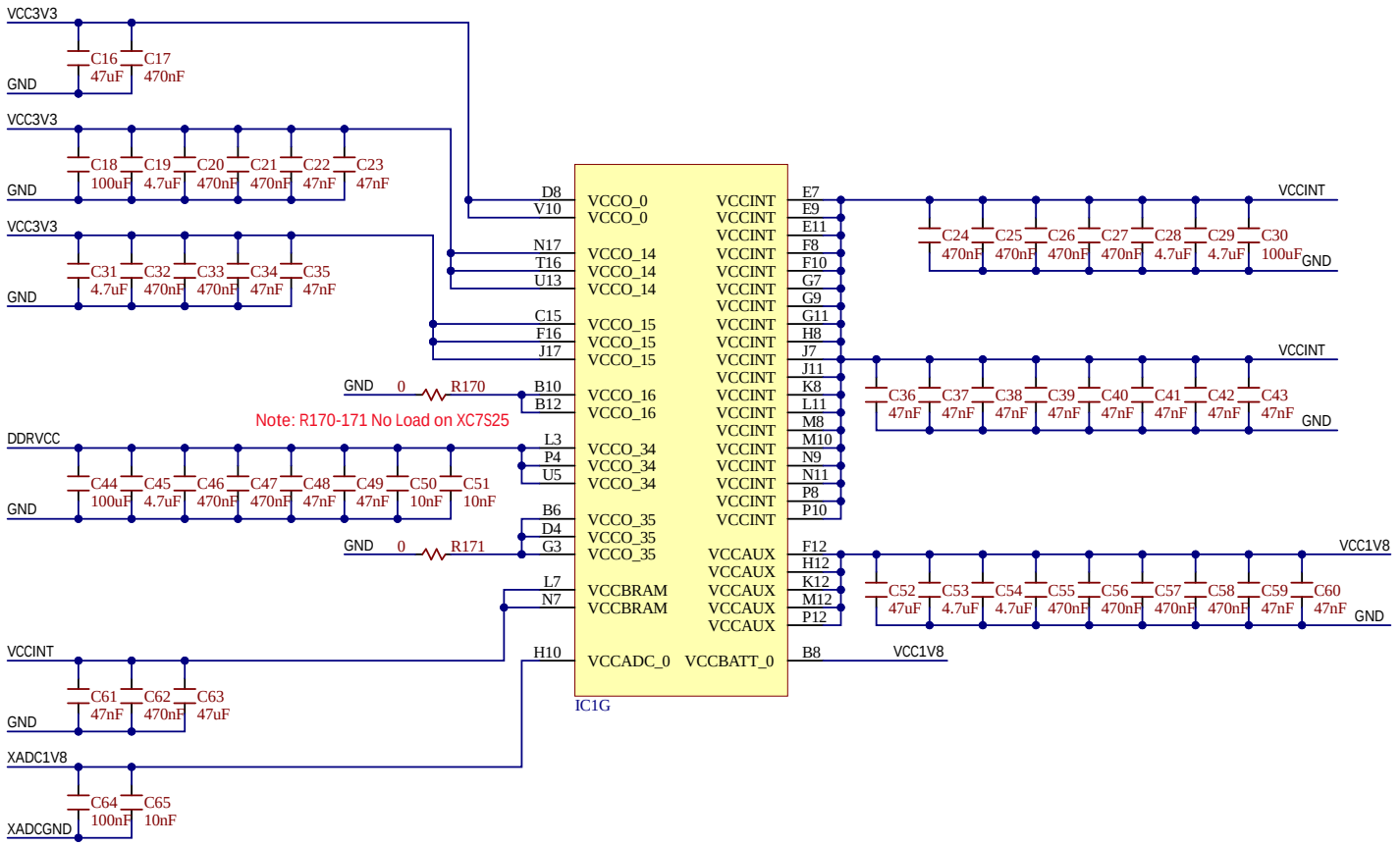

Title	Arty S7
Rev	E.2
Circuit	FPGA Power
Doc#	500-352
Engineer	MTA
Author	GMA
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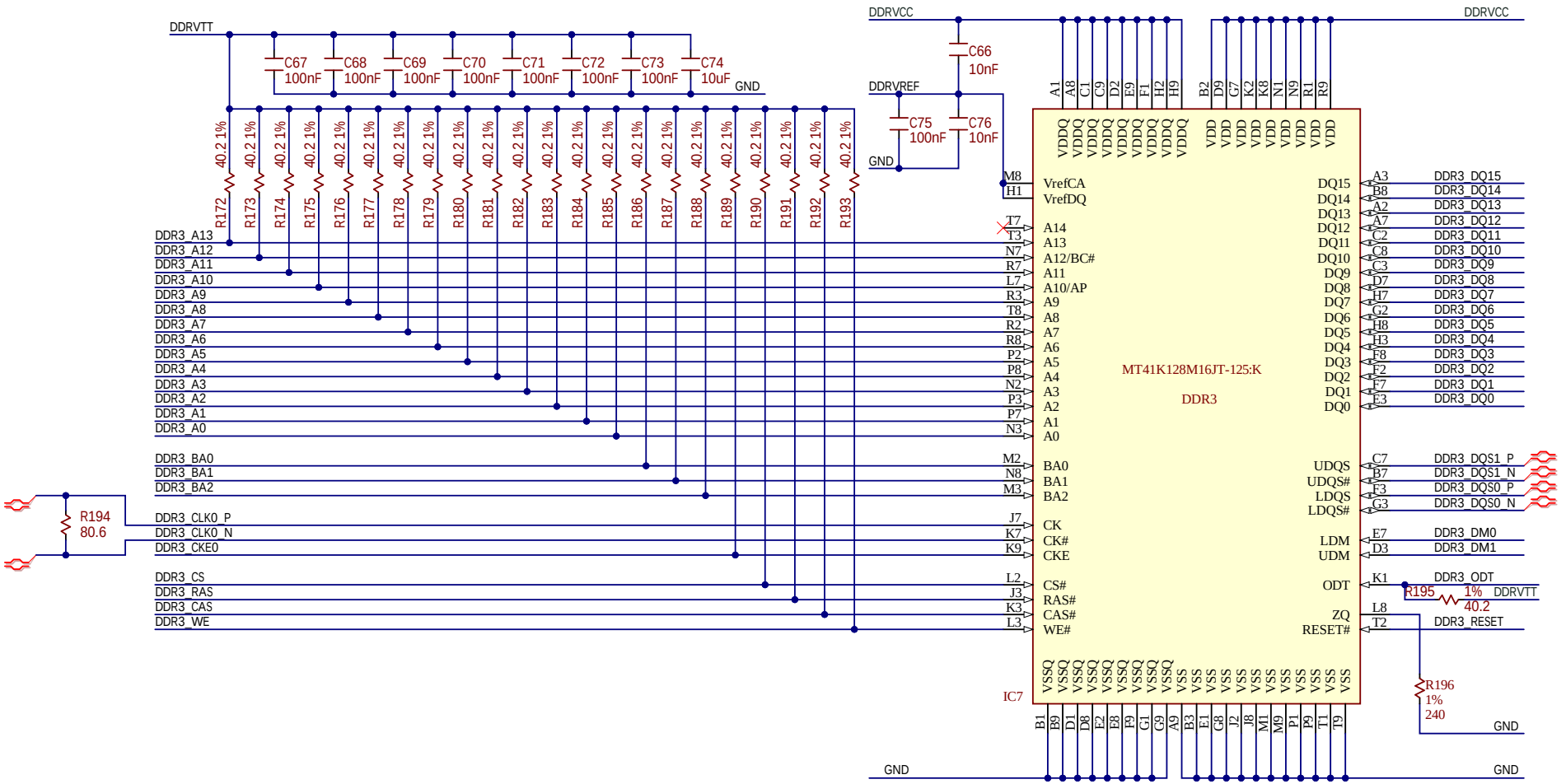

Title	Arty S7
Rev	E.2
Circuit	DDR3
Doc#	500-352
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Title	Arty S7
Rev	E.2
Circuit	USB PROG/UART
Doc#	500-352
Engineer	MTA
Author	GMA
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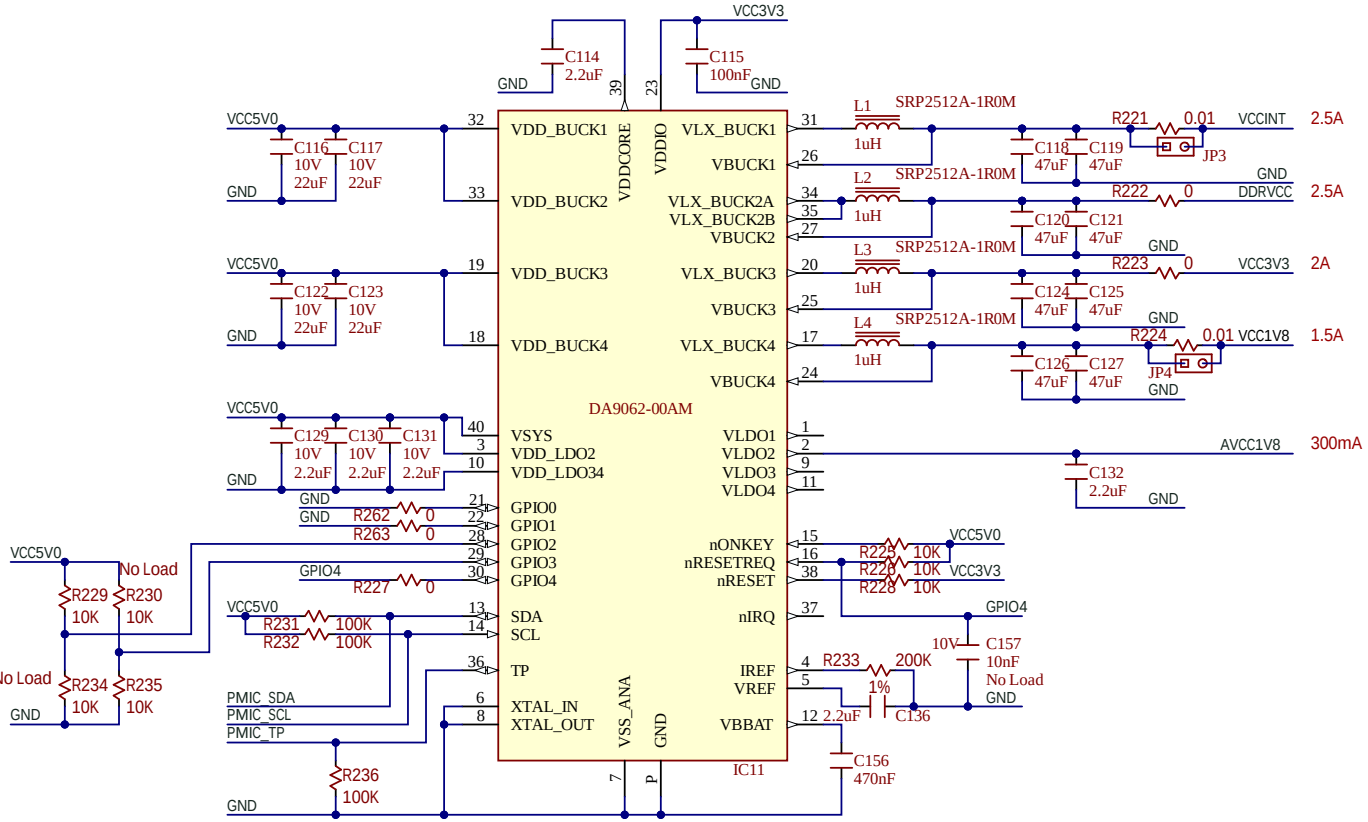

VCCINT Voltage Configuration

R229	R234	VCCINT
Load	No Load	1.0V
No Load	Load	0.95V

DDR Voltage Configuration

R230	R235	DDRVCC	DDRVTT
Load	No Load	1.5V	0.75V
No Load	Load	1.35V	0.675V

Title	Arty S7
Rev	E.2
Circuit	Power Regulation
Doc#	500-352
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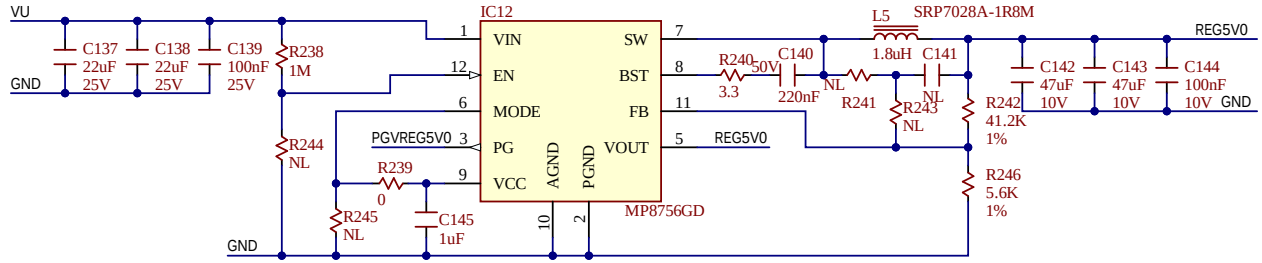

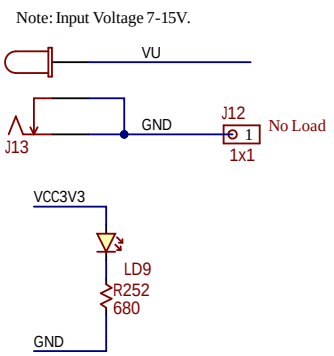

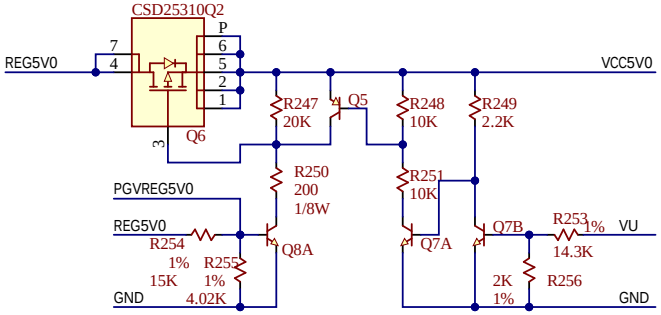

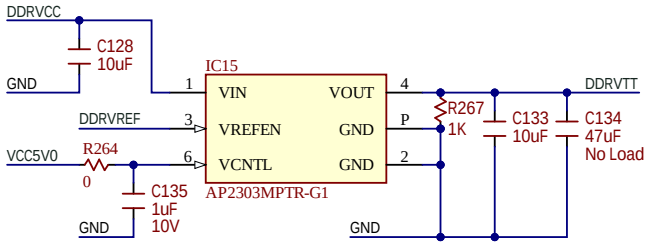

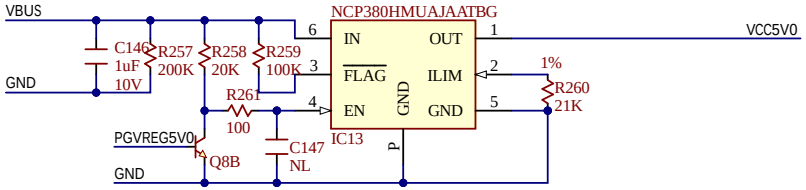

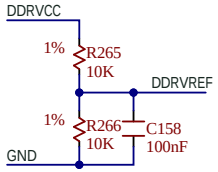

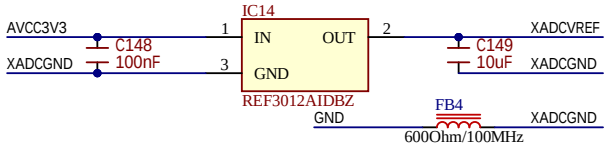

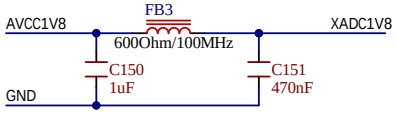

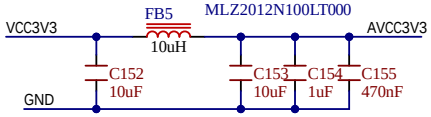

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