

- Foot
- F1
- Foot
- F2
- Foot
- F3
- Foot
- F4

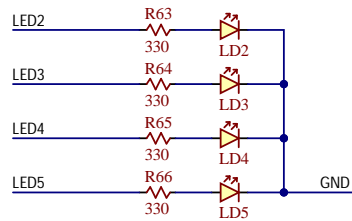
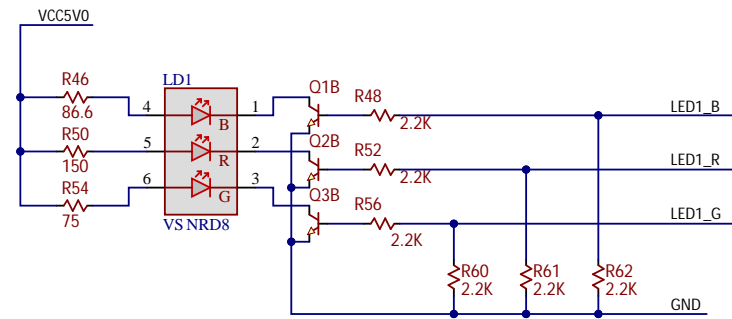
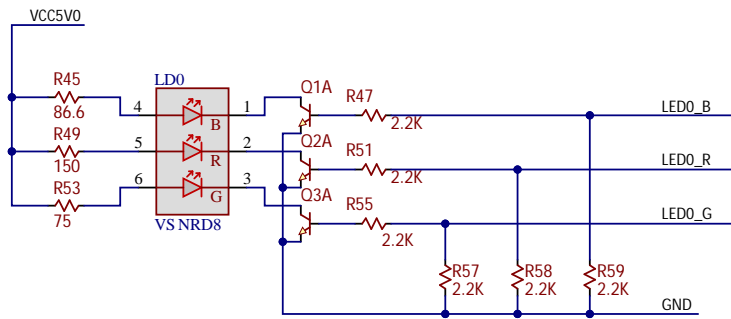
Title		Rev
Arty S7		E.2
Circuit		
PMD, BTN, SWTs		
Doc#	500-352	
Engineer	MTA	
Author	GMA	
Date	1/25/2022	
Sheet#	1 out of 11	



Copyright 2022

Arty S7

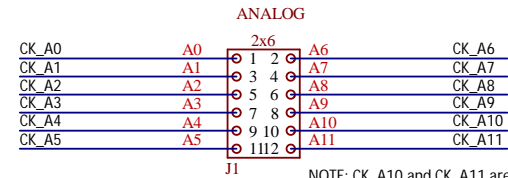
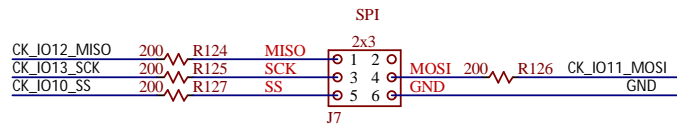
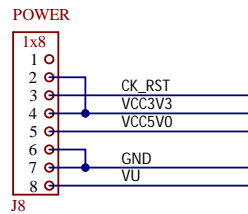
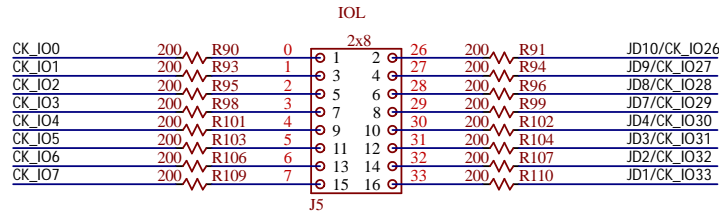
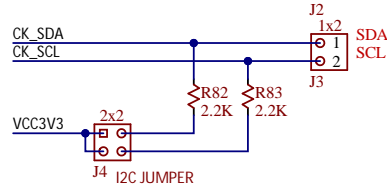
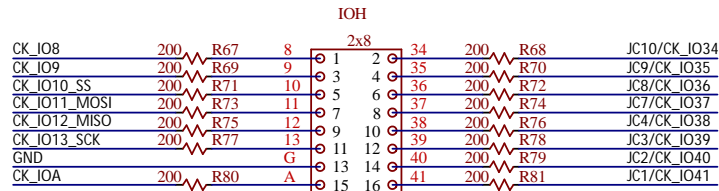
Xilinx    Digilent Inc.    CE    ROHS    Chinese ROHS



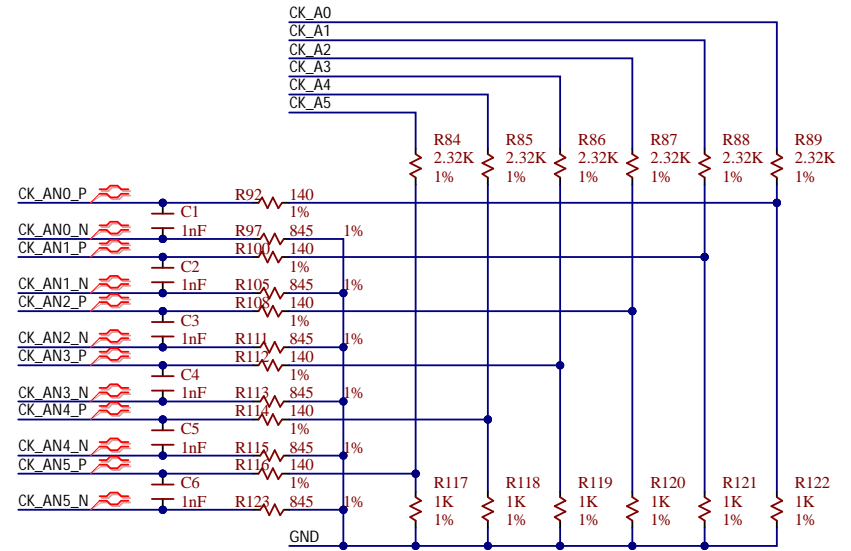
Title		Rev
Arty S7		E.2
Circuit LEDs		
Doc#	500-352	
Engineer	MTA	
Author	GMA	
Date	1/25/2022	
Sheet#	2 out of 11	



Copyright 2022



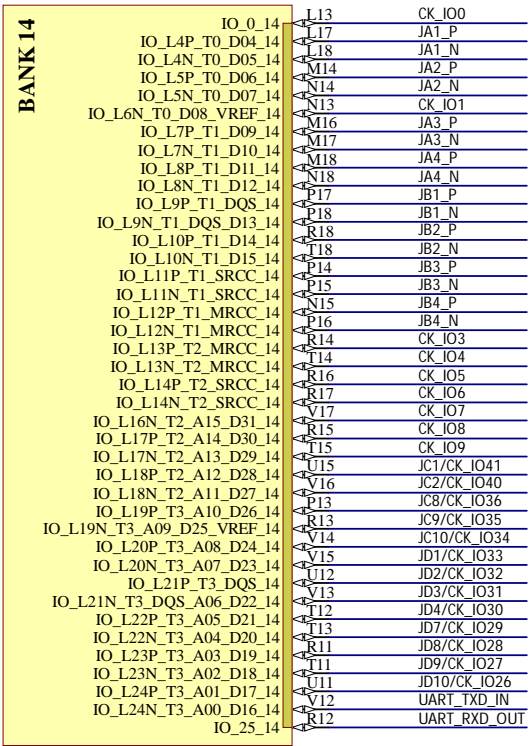
NOTE: CK\_A10 and CK\_A11 are Digital I/O only on XC7550



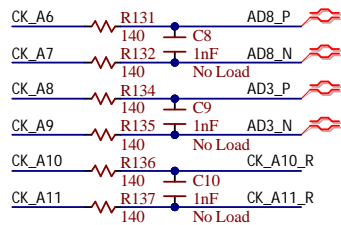
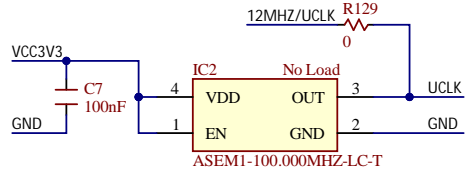
Note: Terminate N signals next to Analog Header

Title		Rev
Arty S7		E.2
Circuit		
CHipKIT IO		
Doc#	500-352	
Engineer	MTA	
Author	GMA	
Date	1/25/2022	
Sheet#	3	out of 11

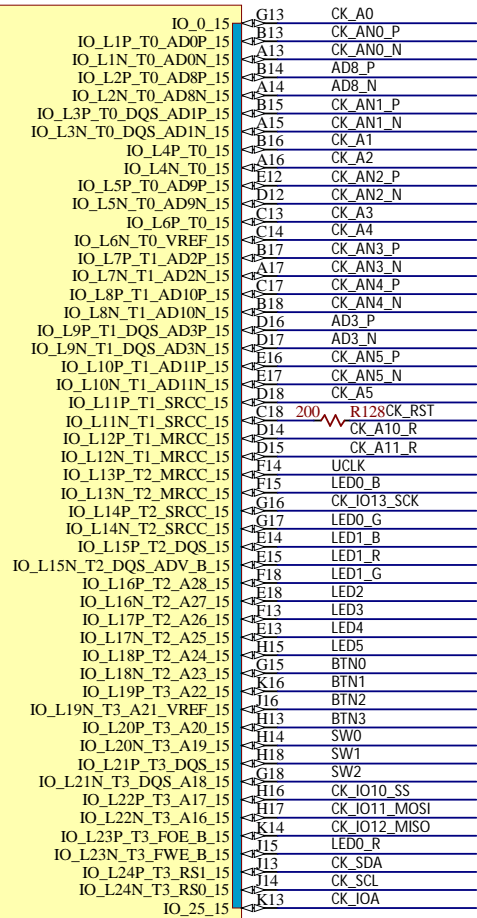
Copyright 2022



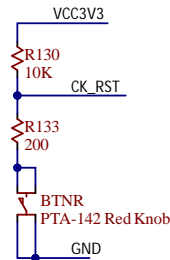
IC1B



**BANK 15**



IC1C



Net Name	XC7S50 XADC	XC7S25 XADC	PIN NAME
CK_AN0_P	Vaux0_v_p	Vaux0_v_p	B13
CK_AN0_N	Vaux0_v_n	Vaux0_v_n	A13
AD8_P	Vaux8_v_p	Vaux8_v_p	B14
AD8_N	Vaux8_v_n	Vaux8_v_n	A14
CK_AN1_P	Vaux1_v_p	Vaux1_v_p	B15
CK_AN1_N	Vaux1_v_n	Vaux1_v_n	A15
CK_AN2_P	Vaux9_v_p	Vaux2_v_p	E12
CK_AN2_N	Vaux9_v_n	Vaux2_v_n	D12
CK_AN3_P	Vaux2_v_p	Vaux10_v_p	B17
CK_AN3_N	Vaux2_v_n	Vaux10_v_n	A17
CK_AN4_P	Vaux10_v_p	Vaux3_v_p	C17
CK_AN4_N	Vaux10_v_n	Vaux3_v_n	B18
AD3_P	Vaux3_v_p	Vaux11_v_p	D16
AD3_N	Vaux3_v_n	Vaux11_v_n	D17
CK_AN5_P	Vaux11_v_p	Vaux4_v_p	E16
CK_AN5_N	Vaux11_v_n	Vaux4_v_n	E17
CK_A10_R	NA	Vaux5_v_p	D14
CK_A11_R	NA	Vaux5_v_n	D15

Arty S7

Rev E.2

Circuit	FPGA Banks
Doc#	500-352
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	4 out of 11

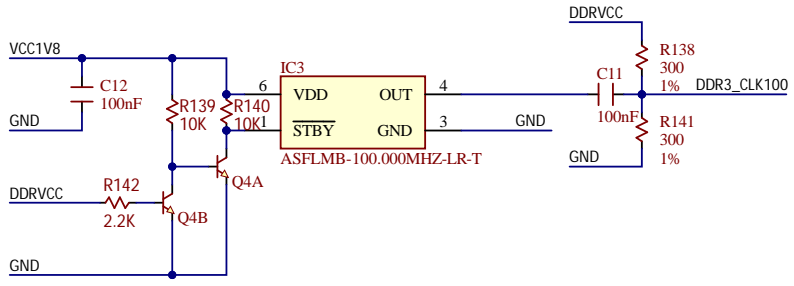


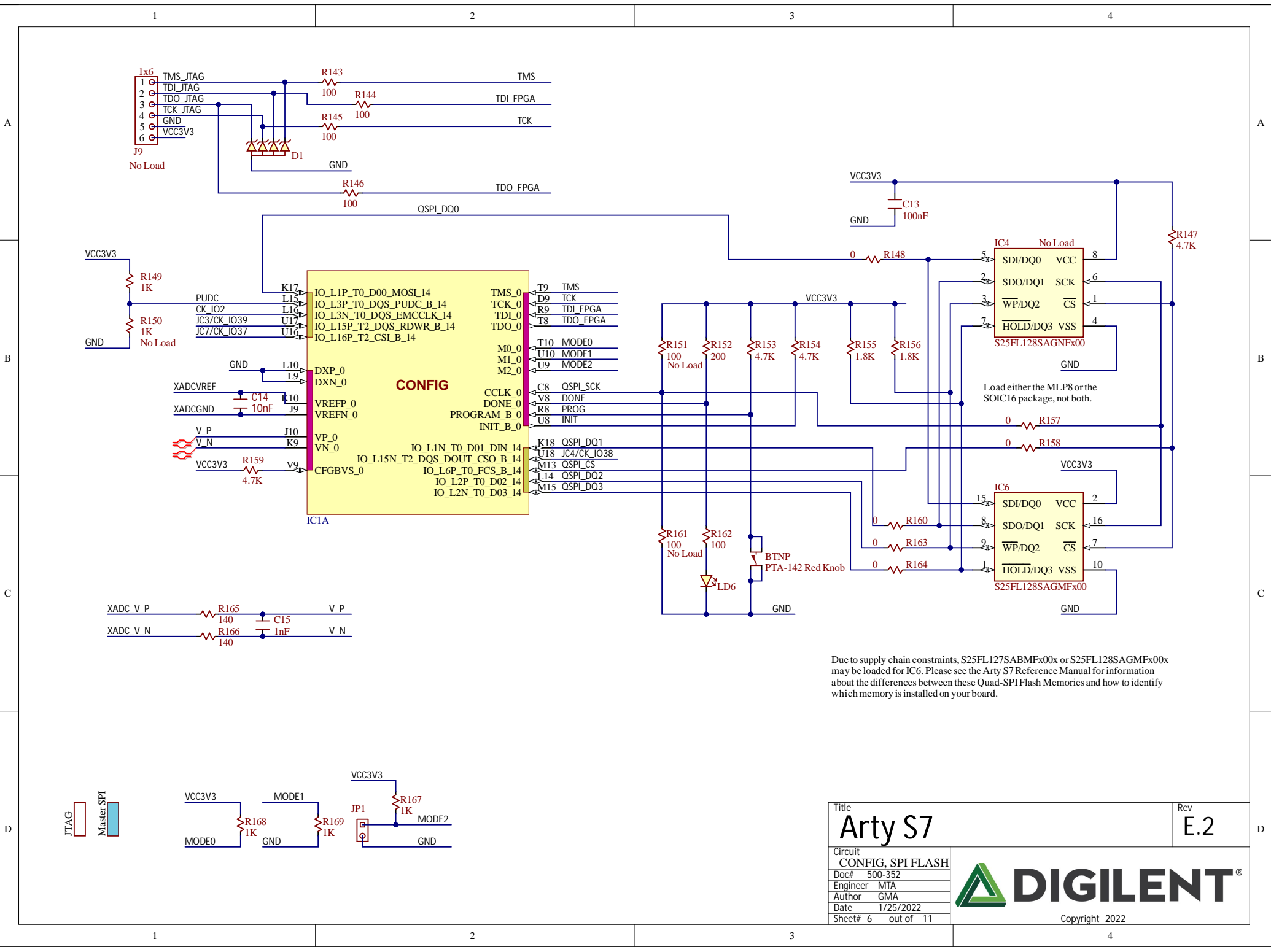
Copyright 2022

**BANK 34**

IO_0_34	J6	DDR3_RESET
IO_L1P_T0_34	K4	DDR3_DM0
IO_L1N_T0_34	L4	DDR3_DQ2
IO_L2P_T0_34	K3	DDR3_DQ1
IO_L2N_T0_34	K2	DDR3_DQ0
IO_L3P_T0_DQS_34	K1	DDR3_DQS0_P
IO_L3N_T0_DQS_34	L1	DDR3_DQS0_N
IO_L4P_T0_34	K6	DDR3_DQ4
IO_L4N_T0_34	L6	DDR3_DQ7
IO_L5P_T0_34	L5	DDR3_DQ6
IO_L5N_T0_34	M4	DDR3_DQ5
IO_L6P_T0_34	M6	DDR3_DQ3
IO_L6N_T0_VREF_34	M5	SW3
IO_L7P_T1_34	M2	DDR3_DM1
IO_L7N_T1_34	M2	DDR3_DQ12
IO_L8P_T1_34	M1	DDR3_DQ14
IO_L8N_T1_34	N1	DDR3_DQ10
IO_L9P_T1_DQS_34	N3	DDR3_DQS1_P
IO_L9N_T1_DQS_34	N2	DDR3_DQS1_N
IO_L10P_T1_34	N5	DDR3_DQ11
IO_L10N_T1_34	N4	DDR3_DQ8
IO_L11P_T1_SRCC_34	P2	DDR3_DQ15
IO_L12P_T1_MRCC_34	P1	DDR3_DQ13
IO_L12N_T1_MRCC_34	R2	DDR3_CLK100
IO_L13P_T2_MRCC_34	R1	DDR3_DQ9
IO_L13N_T2_MRCC_34	R3	DDR3_CS
IO_L14P_T2_SRCC_34	T2	DDR3_CKE0
IO_L14N_T2_SRCC_34	T1	DDR3_BA1
IO_L15P_T2_DQS_34	U1	DDR3_RAS
IO_L15N_T2_DQS_34	U3	DDR3_BA2
IO_L16P_T2_34	U2	DDR3_A0
IO_L16N_T2_34	V3	DDR3_CAS
IO_L17P_T2_34	V2	DDR3_A2
IO_L17N_T2_34	V5	DDR3_BA0
IO_L18P_T2_34	V4	DDR3_A3
IO_L18N_T2_34	R4	DDR3_A1
IO_L19P_T3_34	T3	DDR3_A4
IO_L19N_T3_VREF_34	P6	DDR3_A10
IO_L20P_T3_34	P5	DDR3_ODT
IO_L20N_T3_34	V7	DDR3_A9
IO_L21P_T3_DQS_34	V6	DDR3_A6
IO_L21N_T3_DQS_34	R5	DDR3_CLK0_P
IO_L22P_T3_34	T4	DDR3_CLK0_N
IO_L22N_T3_34	T6	DDR3_A7
IO_L23P_T3_34	T5	DDR3_A11
IO_L23N_T3_34	R7	DDR3_A5
IO_L24P_T3_34	R6	DDR3_A12
IO_L24N_T3_34	U7	DDR3_A8
IO_25_34	U6	DDR3_A13
	P7	DDR3_WE

IC1E



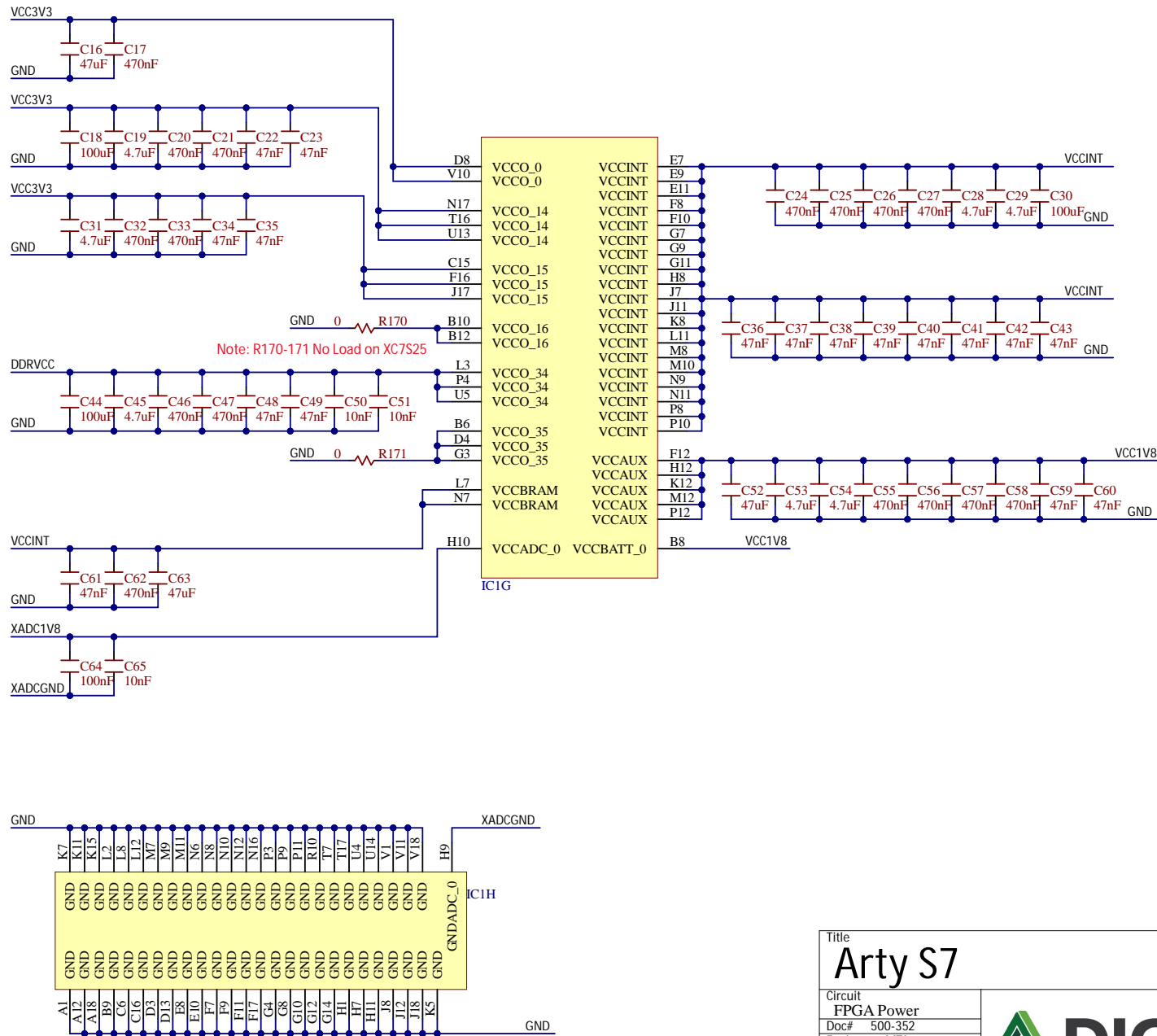


Due to supply chain constraints, S25FL127SABMFx00x or S25FL128SAGMFx00x may be loaded for IC6. Please see the Arty S7 Reference Manual for information about the differences between these Quad-SPI Flash Memories and how to identify which memory is installed on your board.

Title		Rev
Arty S7		E.2
Circuit		
CONFIG, SPI FLASH		
Doc# 500-352		
Engineer MTA		
Author GMA		
Date 1/25/2022		
Sheet# 6 out of 11		



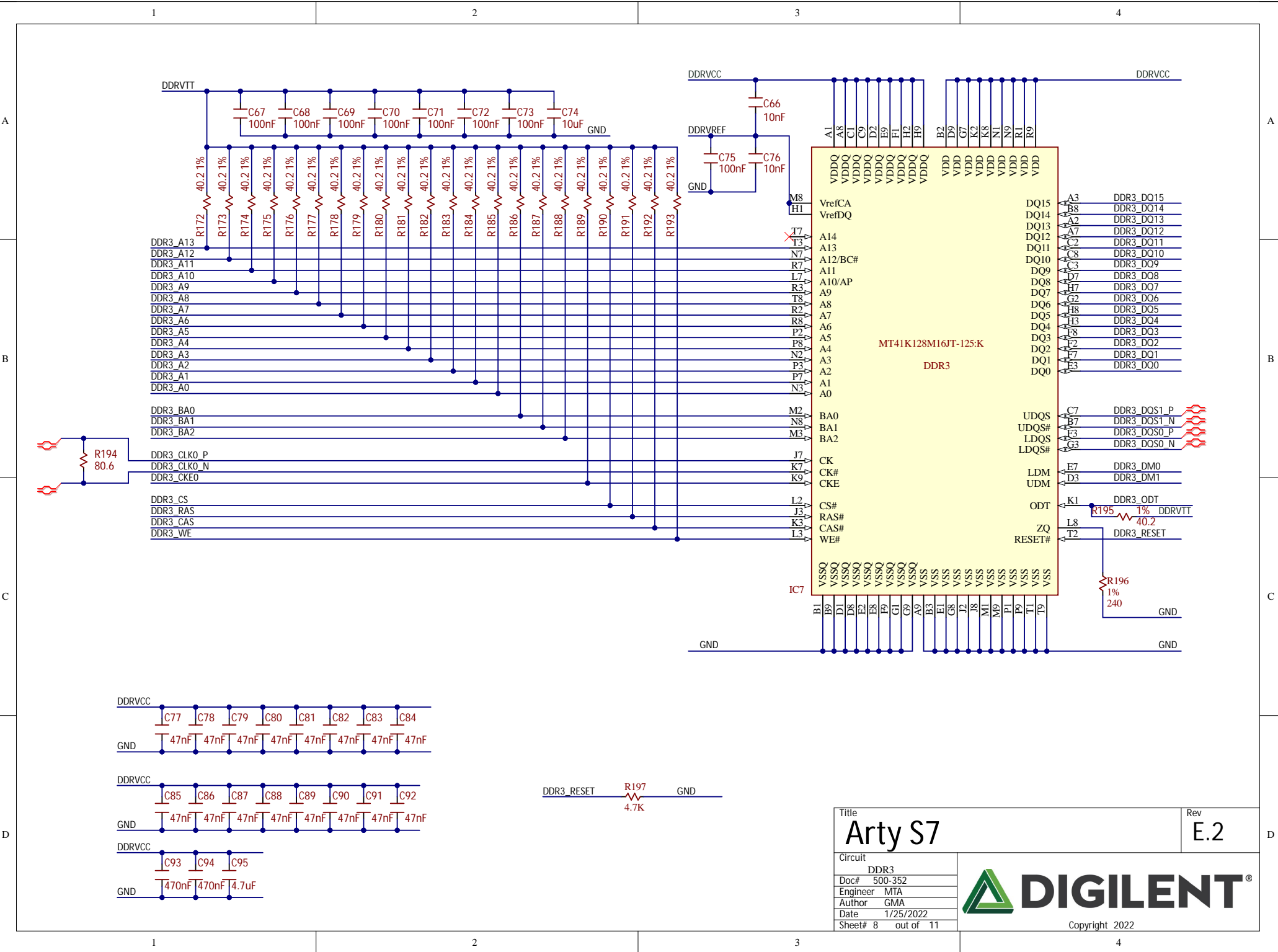
Copyright 2022



Title		Rev
<b>Arty S7</b>		<b>E.2</b>
Circuit	FPGA Power	
Doc#	500-352	
Engineer	MTA	
Author	GMA	
Date	1/25/2022	
Sheet#	7	out of 11



Copyright 2022



Title		Rev
Arty S7		E.2
Circuit		
DDR3		
Doc# 500-352		
Engineer MTA		
Author GMA		
Date 1/25/2022		
Sheet# 8 out of 11		

Copyright 2022



1

2

3

4

A

A

B

B

C

C

D

D

This page intentionally left blank.

Title		Rev	
Arty S7		E.2	
Circuit			
USB PROG/UART			
Doc#	500-352		
Engineer	MTA		
Author	GMA		
Date	1/25/2022		
Sheet#	9 out of 11		



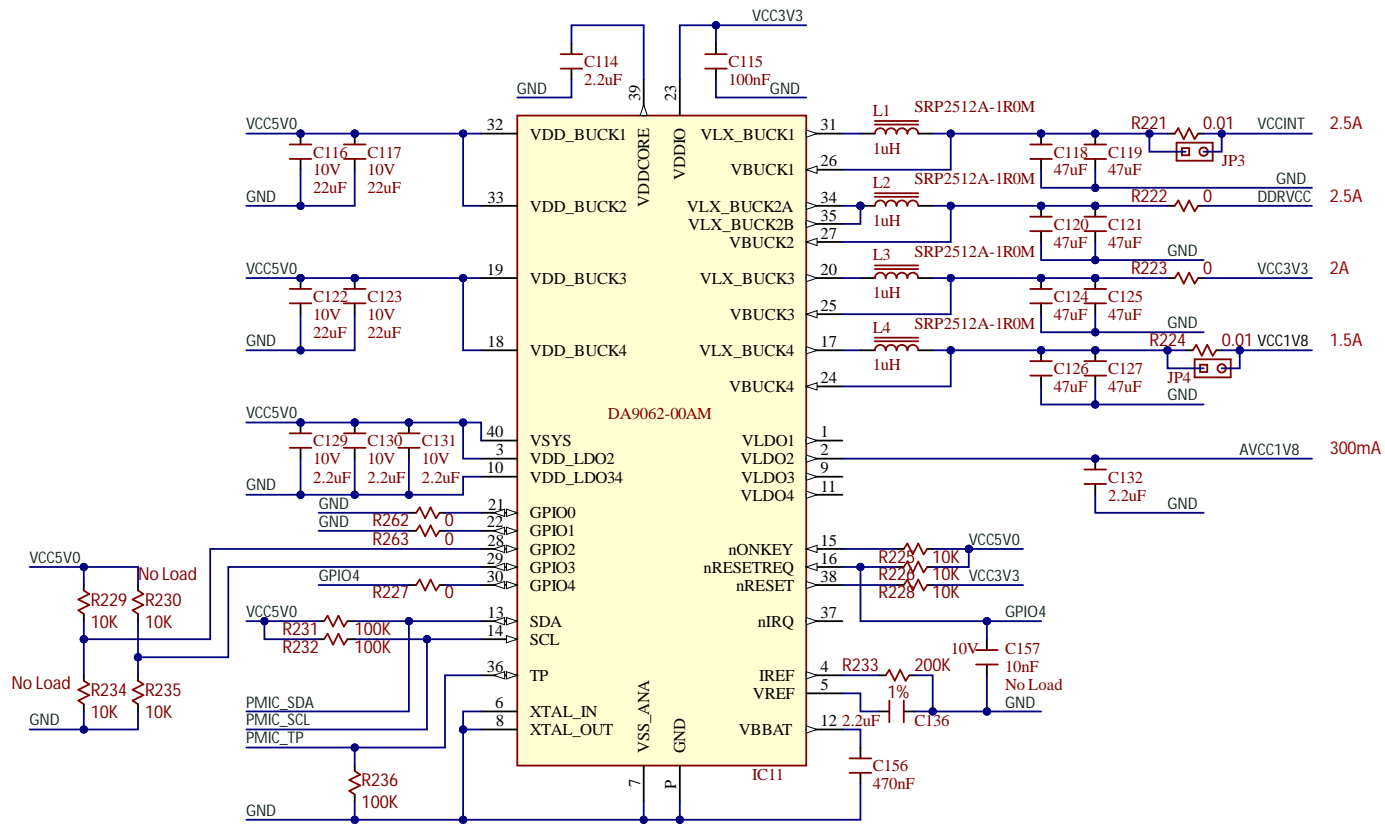
Copyright 2022

1

2

3

4

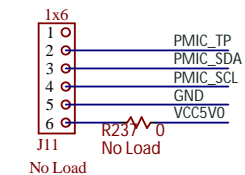


VCCINT Voltage Configuration

R229	R234	VCCINT
Load	No Load	1.0V
No Load	Load	0.95V

DDR Voltage Configuration

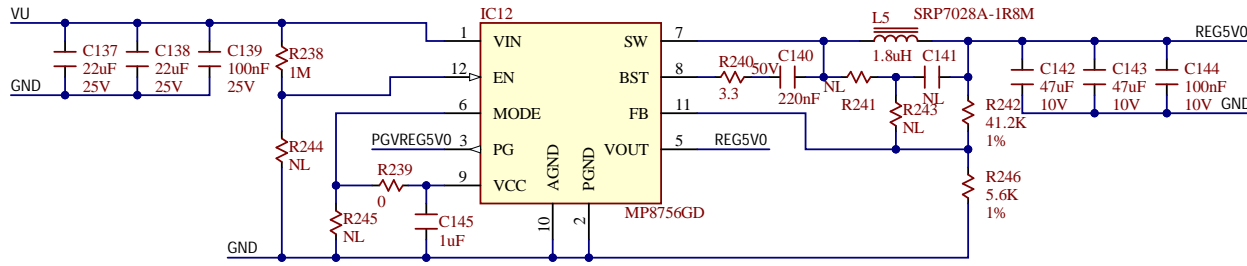
R230	R235	DDRVC	DDRVTT
Load	No Load	1.5V	0.75V
No Load	Load	1.35V	0.675V



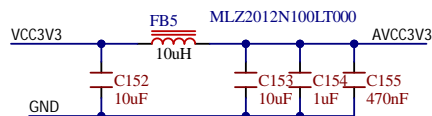
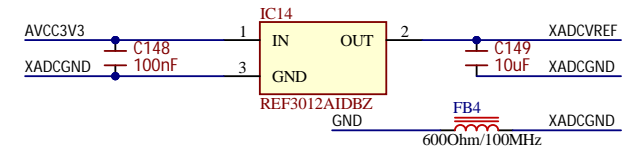
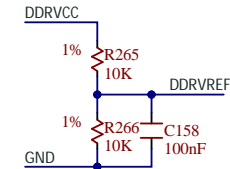
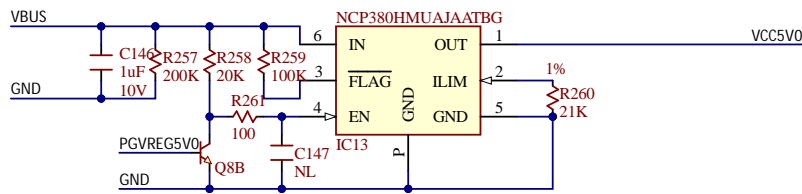
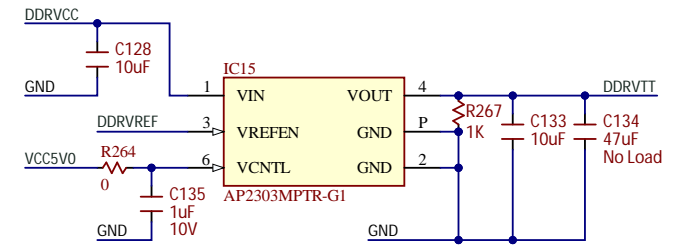
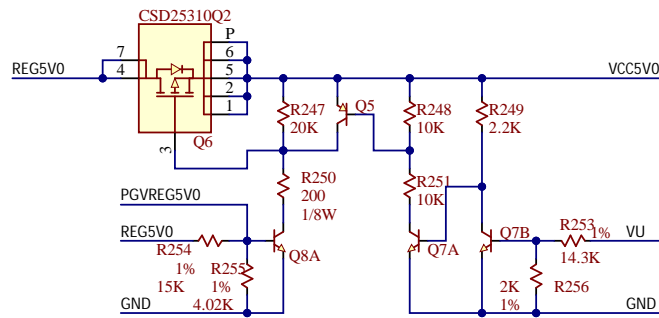
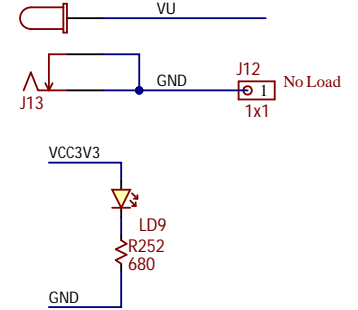
Title <b>Arty S7</b>		Rev <b>E.2</b>
Circuit Power Regulation		
Doc# 500-352		
Engineer MTA		
Author GMA		
Date 1/25/2022		
Sheet# 10 out of 11		



Copyright 2022



Note: Input Voltage 7-15V.



Title		Rev
Arty S7		E.2
Circuit		
Power Regulation		
Doc# 500-352		
Engineer MTA		
Author GMA		
Date 1/25/2022		
Sheet# 11 out of 11		



Copyright 2022