

6.3.2: Leakage Currents and Electrolytic Capacitors

Overview:

Voltage-current relationships for ideal capacitors do not always adequately explain measured capacitor behavior. In this assignment, we will focus on the effects of *leakage currents* on capacitor behavior. As we saw in our discussion of non-ideal capacitors in section 6.3 of the text, models for realistic capacitors often include a resistor in parallel with an ideal capacitor; this resistor allows us to model leakage currents, which explain – among other effects – the inability of a capacitor to hold a charge indefinitely, even if the capacitor terminals are open-circuited.

An important effect of leakage currents is in the case of *electrolytic* capacitors. These capacitors are attractive in many cases, since a relatively large capacitance can be provided in a small package. However, one must be aware, when using electrolytic capacitors, that their leakage currents can be significant and that they are not symmetric relative to the capacitor's polarity. Thus, reversing the polarity of the capacitor in a circuit can alter the behavior of the capacitor – this makes electrolytic capacitors undesirable in some applications (such as filtering) in which the behavior of the capacitor should be independent of the polarity of the voltage applied to the capacitor.

Before beginning this lab, you should be able to:

- State voltage-current relationships for capacitors in both differential and integral form
- Define the time constant of an exponential waveform
- Use the Analog Discovery to apply and measure time-varying waveforms (Lab 6.2.1)

After completing this lab, you should be able to:

- Model a non-ideal capacitor as an ideal capacitor in parallel with a resistor
- Identify some effects of non-ideal capacitors
- Describe how the polarity of an electrolytic capacitor affects the capacitor's leakage current.

This lab exercise requires:

- Analog Discovery module
- Diligent Analog Parts Kit

Symbol Key:

	Demonstrate circuit operation to teaching assistant; teaching assistant should initial lab notebook and grade sheet, indicating that circuit operation is acceptable.
	Analysis; include principle results of analysis in laboratory report.
	Numerical simulation (using PSPICE or MATLAB as indicated); include results of MATLAB numerical analysis and/or simulation in laboratory report.
	Record data in your lab notebook.

General Discussion:

In large part, this lab will be concerned with *electrolytic* capacitors. Electrolytic capacitors are polarized – that is, one of their terminals is intended to always be at a higher voltage than the other. The terminal which is intended to be at the higher voltage is called the *anode*, while the terminal which is to be at the lower polarity is the *cathode*. A symbol for an electrolytic capacitor is shown in Figure 1 – the cathode side is indicated as a curved line. Physically, electrolytic capacitors are readily identifiable: the lead connected to the anode is a longer wire than that of the cathode, and (if the capacitor is physically large enough) a bar is printed on the cathode side of the capacitor¹.

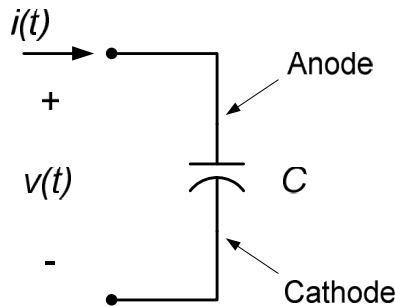


Figure 1. Electrolytic capacitor circuit symbol.

Electrolytic capacitors are desirable in that their capacitance can be large relative to their volume. However, they also have some undesirable qualities. Chief among these is that they can fail rather spectacularly if the cathode voltage is significantly higher than the anode voltage for an extended period of time. More subtle drawbacks include the fact that leakage currents can be large if the polarity of the capacitor is reversed². It is this latter characteristic that we will explore in this assignment.

Caution:

In order to explore leakage effects, we will be applying voltages with the opposite polarity as required by the electrolytic capacitor. Due to the voltage levels we will use, it is unlikely that we will cause a failure of the capacitor. However, it is recommended that you wear eye protection while doing this lab assignment.

In this lab assignment, we will measure the voltage across an electrolytic capacitor for both of the cases shown in Figure 2. In Figure 2(a), the polarity of the capacitor is correct; the anode is always at the higher voltage. In Figure 2(b), the polarity of the capacitor is reversed – the cathode is now at the higher voltage. We will use a

¹ In addition, the bar may have a negative sign printed on it, which further indicates that the cathode is to be at the lower (or negative) voltage.

² The non-symmetry of the leakage currents relative to capacitor voltage makes electrolytic capacitors poor choices for filter circuits. Filter circuits typically require their operation to be identical for positive and negative voltage inputs, unless special biasing schemes are introduced to ensure that the voltage polarity does not change.

“switch” to change the voltage applied to the capacitor – our switch will be implemented simply by unplugging the positive voltage terminal of our power supply from the rest of the circuit.

The resistor R in the circuit of Figure 2 simply limits the amount of current the capacitor demands when it is being initially charged. Capacitors require a large amount of current to charge rapidly; without the resistor, the capacitor will attempt to draw more current from the power supply than is available.

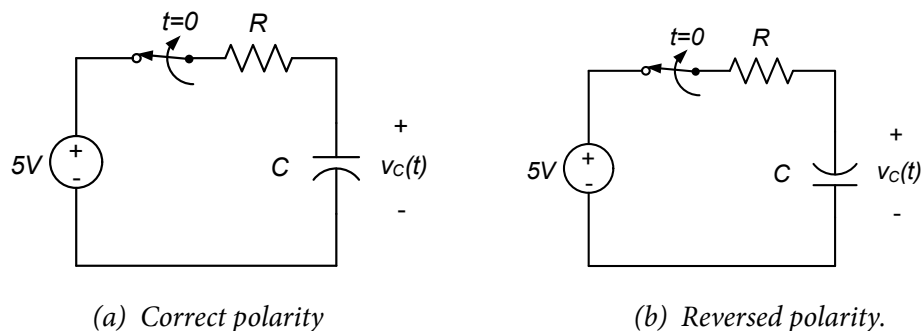


Figure 2. Capacitor configurations used in this lab.

Pre-lab:

None

Lab Procedures:

1. Using $R = 100\Omega$ and $C = 10\mu\text{F}$, implement the circuit of Figure 2(a). (Recall that, in Figure 2(a), the anode is at the higher voltage. Thus, the capacitor terminal with the longer lead is connected to the resistor R and the shorter lead is connected to ground.) Use $V+$ to apply the 5V supply.
 - i. Use channel 1 of your oscilloscope to measure the voltage across the capacitor, $v_C(t)$. We will be monitoring the amount of time required for the capacitor to discharge once we open the switch in Figure 2(a); this will take a relatively long time, so set the time scale on your oscilloscope to 5 s/div. Set the vertical scale of your scope to 1 V/div, with a -2V offset.
 - ii. Turn on the power supply and click  to start acquisition of data. The oscilloscope should indicate a +5V voltage across the capacitor.
 - iii. Open the “switch” in Figure 2(a) by unplugging the power supply terminal from the circuit. (Simply pull the $V+$ connector out of the breadboard.) The capacitor voltage displayed on the oscilloscope screen should decay exponentially. Measure the time constant of the waveform³. Record the image of the oscilloscope window, showing the waveform.
- iv. Demonstrate operation of your circuit to the Teaching Assistant. Have the TA initial the appropriate page(s) of your lab notebook and the lab checklist.

DATA

DEMO

³ Recall that the time constant is the amount of time required for an exponential waveform to decay to 36.8% of its initial value.

2. Still using $R = 100\Omega$ and $C = 10\mu\text{F}$, implement the circuit of Figure 2(b). (In Figure 2(b), the cathode is at the higher voltage. Thus, the capacitor terminal with the shorter lead is connected to the resistor R and the longer lead is connected to ground.) Use $V+$ to apply the 5V supply. Note that this circuit can be easily created from the circuit of Figure 2(a) by removing the capacitor, reversing the leads, and replacing it again.
 - i. Measure the voltage across the capacitor, $v_C(t)$, as in part 1. Turn on the power supply and click  to start acquisition of data. The oscilloscope should indicate a +5V voltage across the capacitor.
 - ii. Open the “switch” in Figure 2(b) by unplugging the power supply terminal from the circuit. (Simply pull the $V+$ connector out of the breadboard.) The capacitor voltage displayed on the oscilloscope screen should decay approximately exponentially. Measure the time constant of the waveform. Record the image of the oscilloscope window, showing the waveform.
3. In the circuits of Figure 2, there is no way for the capacitor’s voltage to decay – the charge difference on the plates cannot “leak” away, since there is (in our model, anyway) no path for the charge to get from one plate to the other. The circuits of Figure 2 are not realistic, based on the capacitor behavior we observed in parts 1 and 2 above. We must modify how we think about capacitors’ behavior in order to explain our data!

DATA

DEMO

In section 6.3 of the textbook, we modeled non-ideal capacitors as a resistance in parallel with an ideal capacitor. Using this model, the circuits of Figure 2 can be modified to become Figure 3 below. Now there is a path – the resistor R_C – which allows the capacitor voltage to decay after the switch opens, allowing us to explain our previous data!

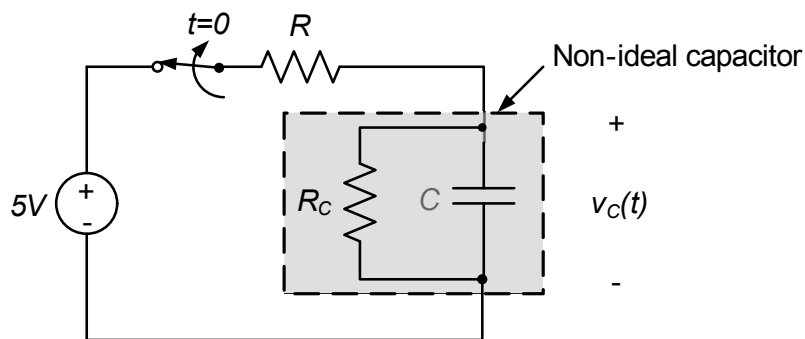


Figure 3. Circuit of Figures 2, with non-ideal capacitor.

As we observed in parts 1 and 2 above, the leakage rate in electrolytic capacitors changes, based on the polarity of the capacitor voltage. In essence, this means that the capacitor resistance, R_C , in the model of Figure 3 depends on the polarity of the capacitor voltage⁴!

⁴ This makes modeling electrolytic capacitors whose voltage changes polarity tedious, to say the least.

To obtain an idea as to the variation in the capacitor resistance when the capacitor polarity is reversed, let's normalize the time constants we measured in parts 1 and 2 above. To do this, simply divide the time constant by the capacitance value:

$$R_C \approx \frac{\tau}{C} \quad (1)$$

As we will see later, the units of equation (1) are consistent.

ANALYSIS

- i. Tabulate the results you obtained in parts 1, 2, and 3 above – for each polarity, list the measured time constant, and the estimated capacitor resistance as determined by equation (1). Briefly comment on the magnitude of these resistances and the differences between the capacitor resistances for the two cases. (Include a percent change in resistance induced by changing the capacitor polarity.)

Post-lab Exercises:

ANALYSIS

Suppose that we modify the circuit of Figure 2(a) so that there is a path for the capacitor to dissipate its voltage after the switch opens, as shown in Figure 4. Based on the capacitor resistances you estimated in part (c) of the lab procedures, how large would the resistor R need to be in order for the capacitor resistance R_C to change the rate at which the capacitor voltage dissipates by about 10%? (E.g. how large would R need to be before the measured time constant of the capacitor voltage decay changes by 10% when the resistance R_C is included?)

Hint: the resistances R and R_C are in parallel. They can be combined to a single equivalent resistance seen by the capacitor.

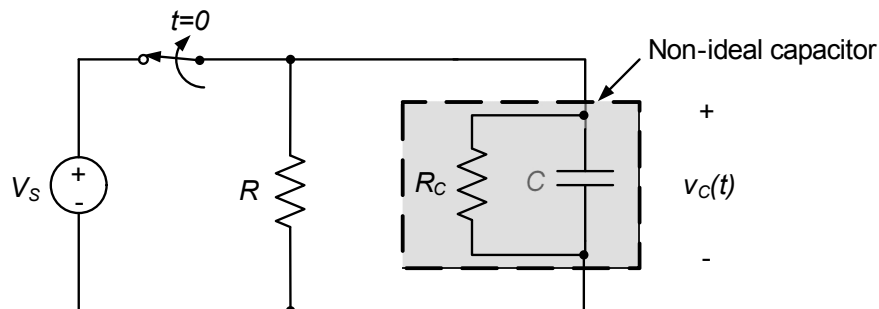


Figure 4. Circuit with external resistor connected across non-ideal capacitor.