

A

B

C

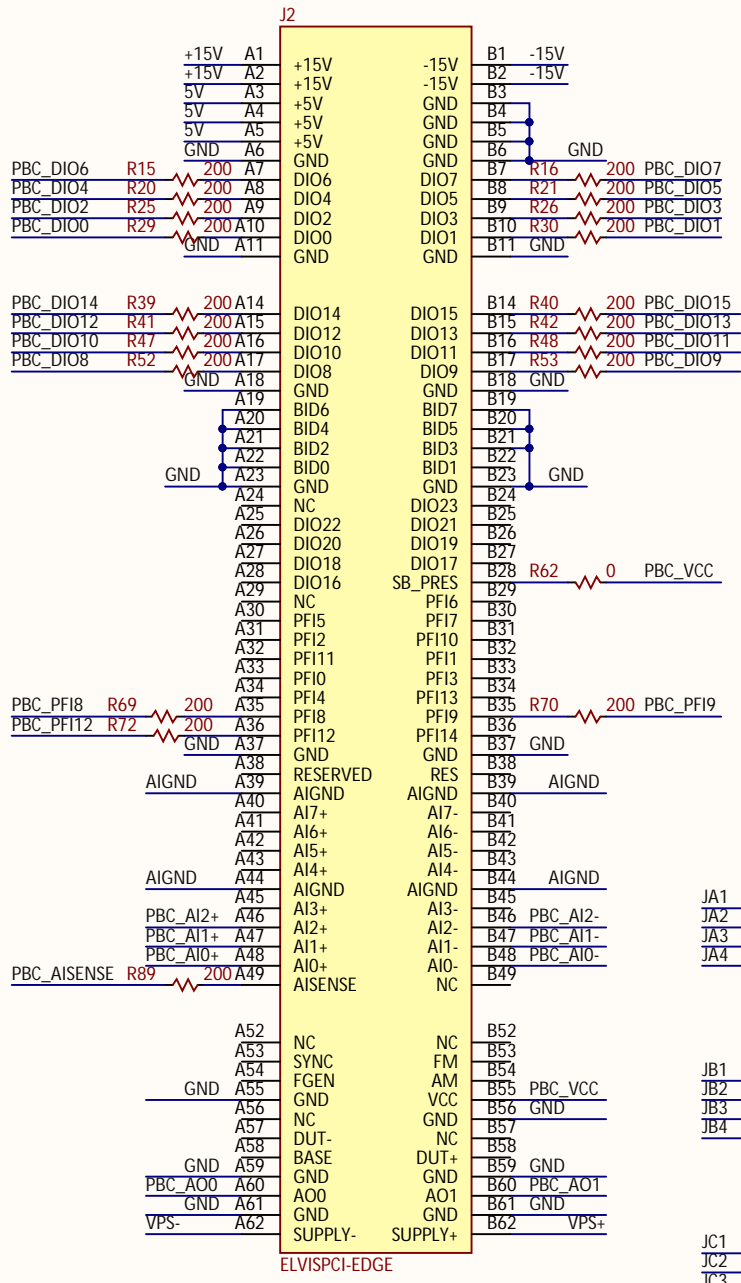
D

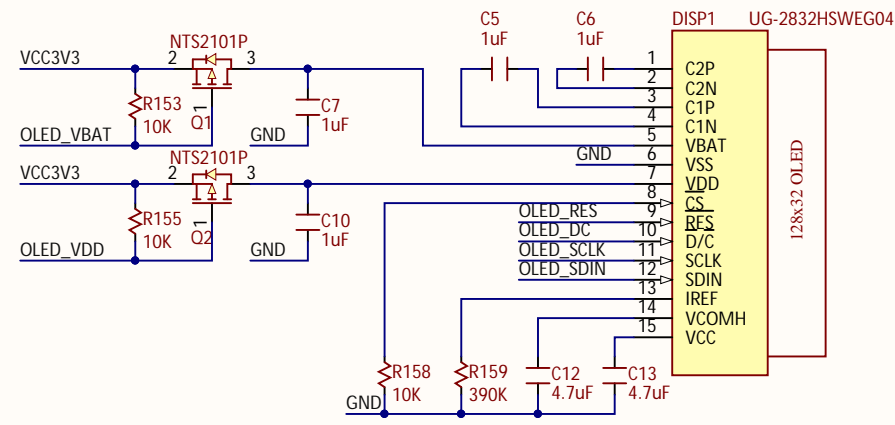
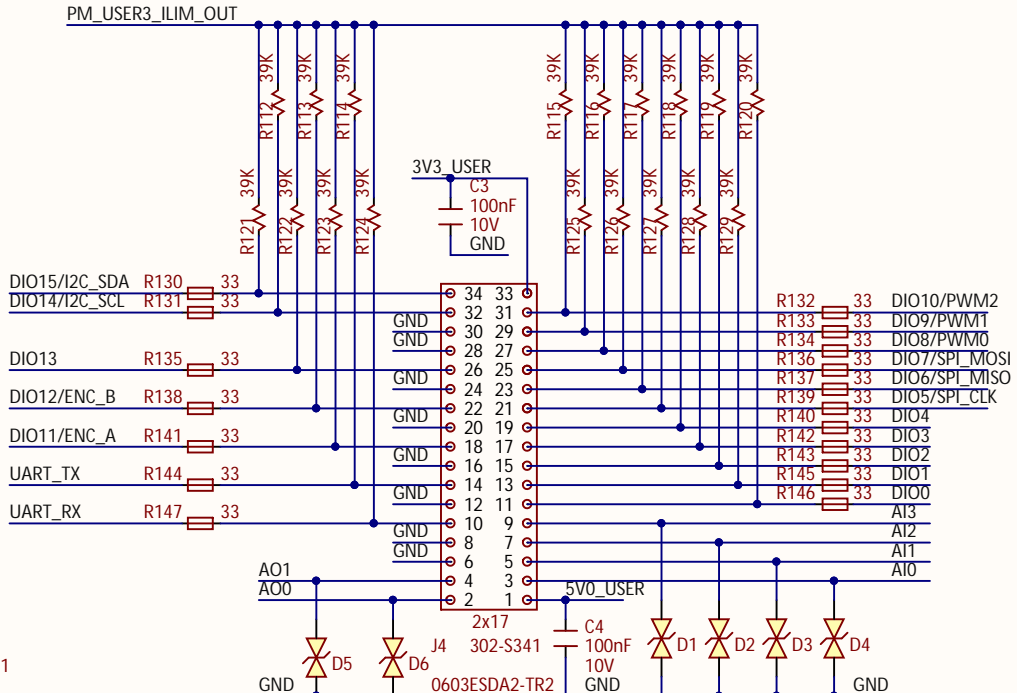
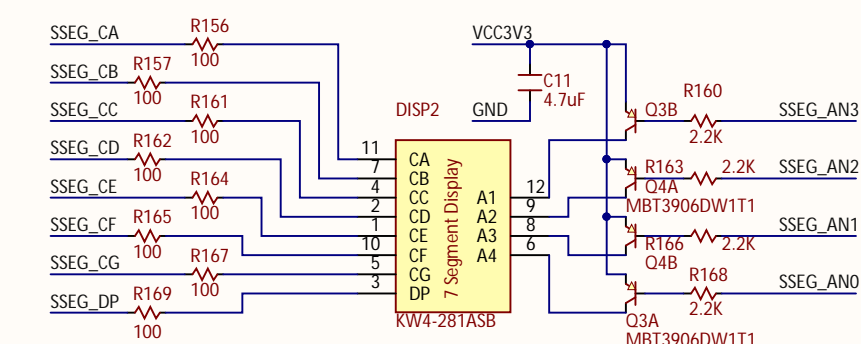
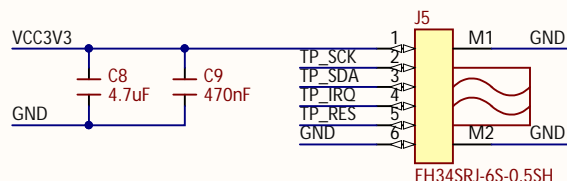
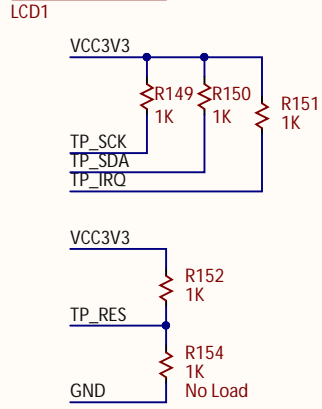
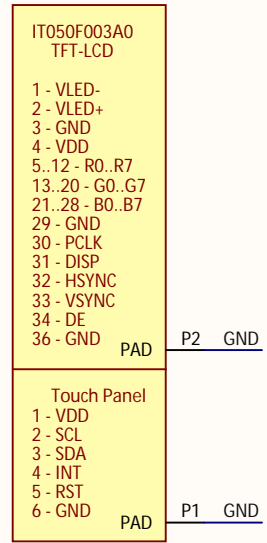
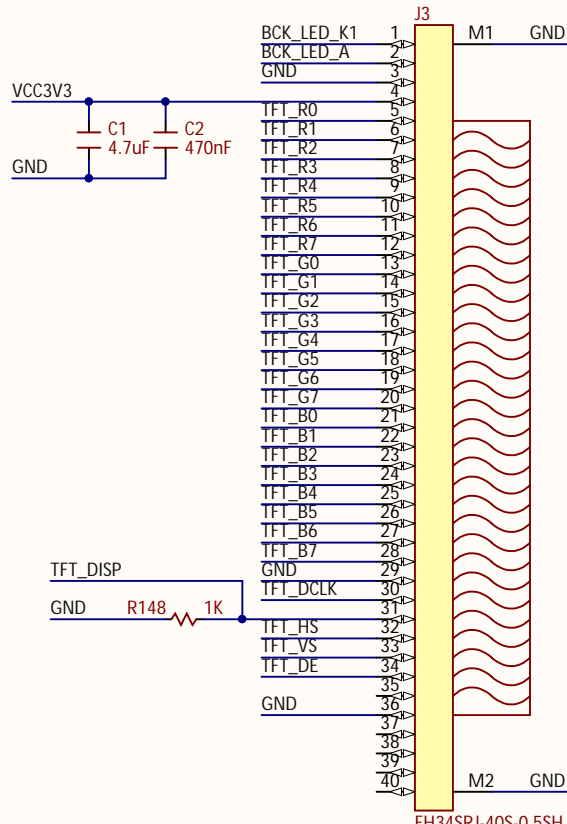
A

B

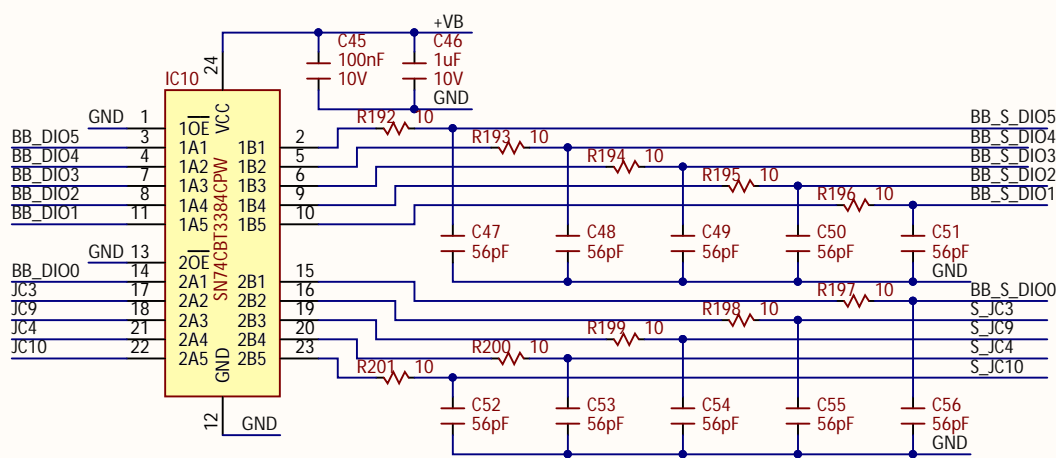
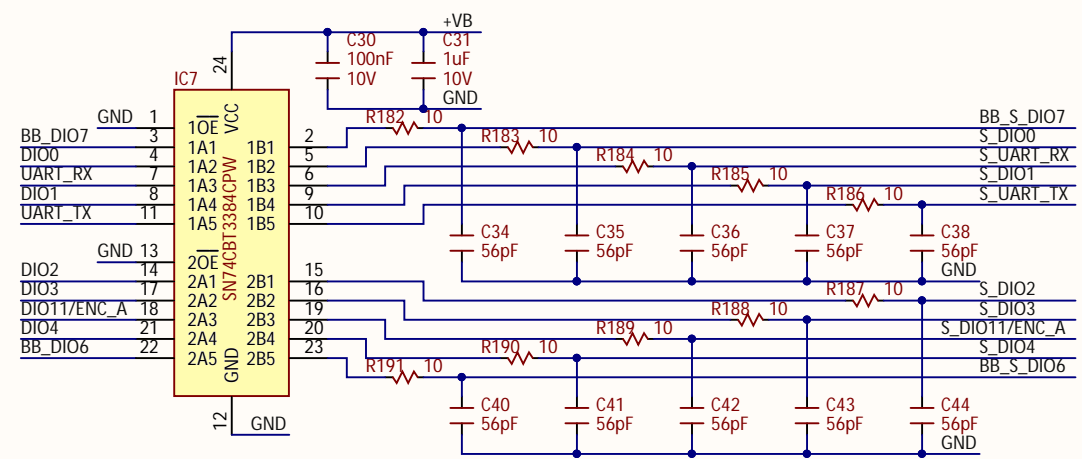
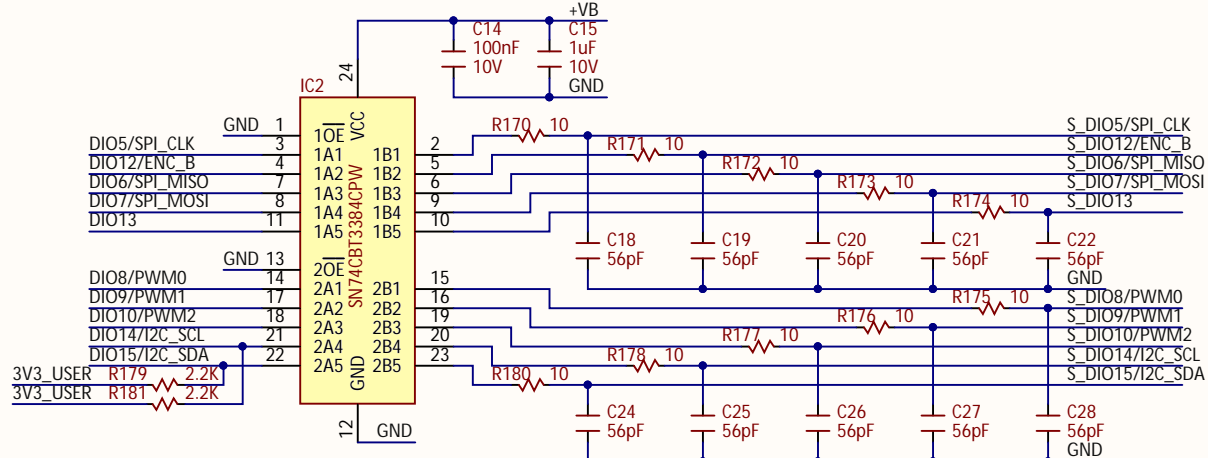
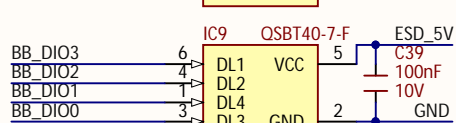
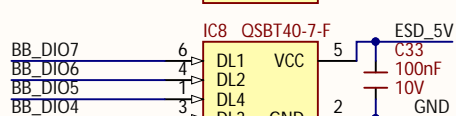
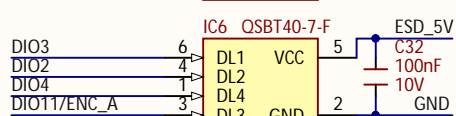
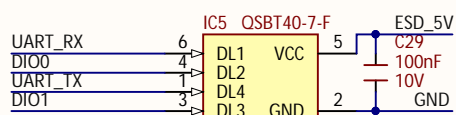
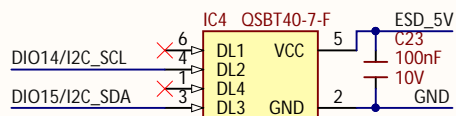
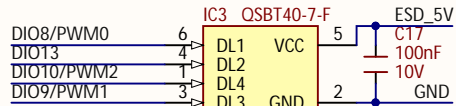
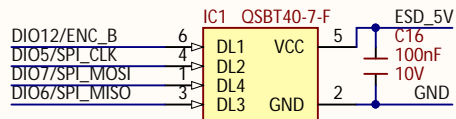
C

D

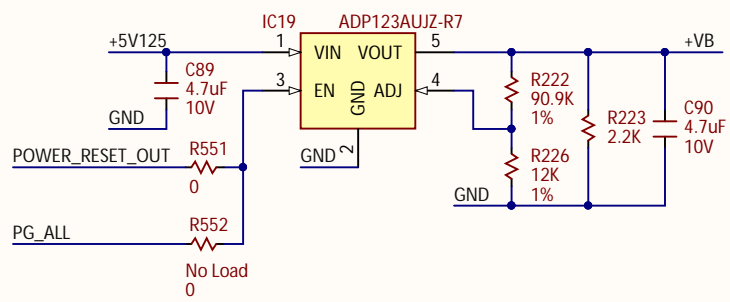
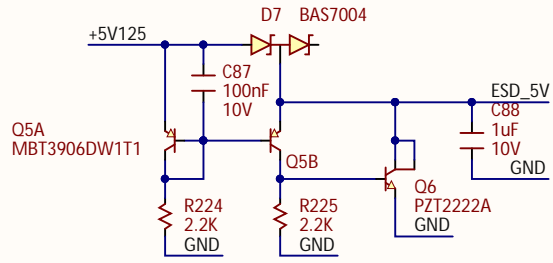
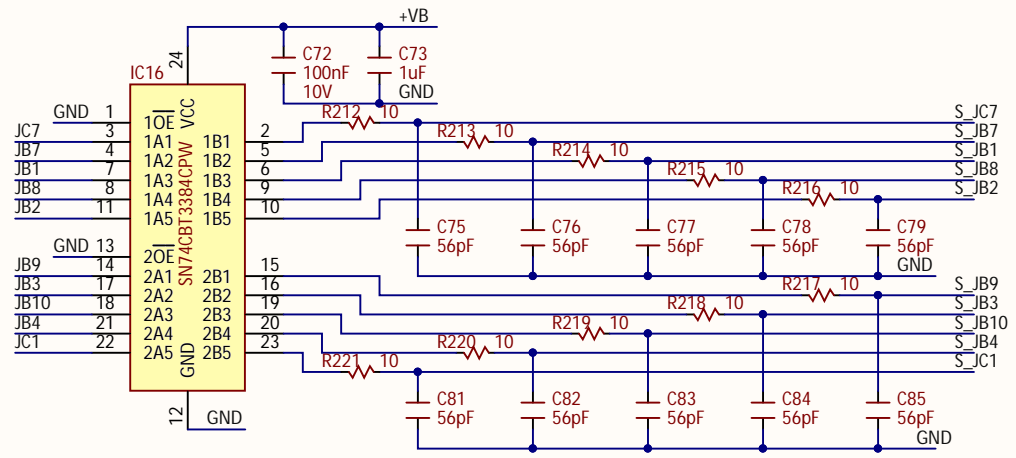
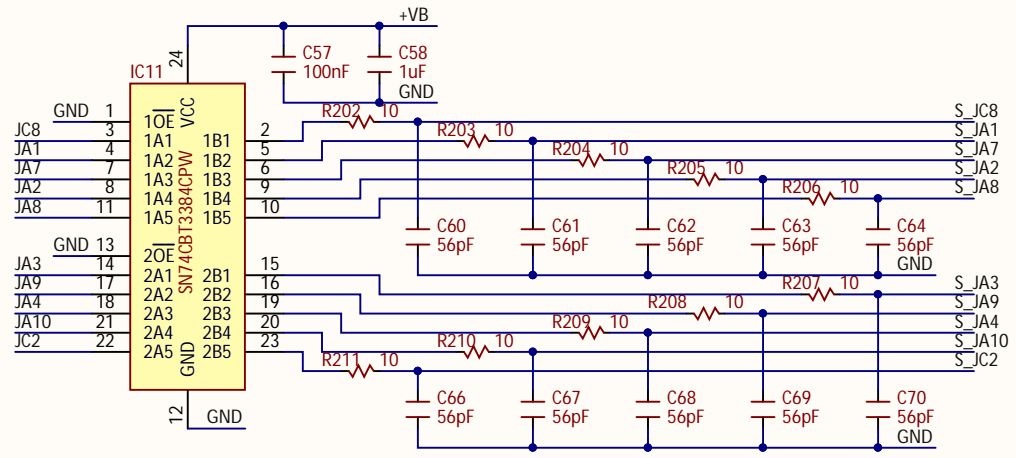
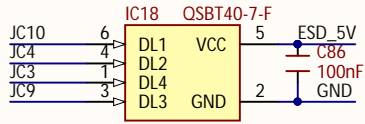
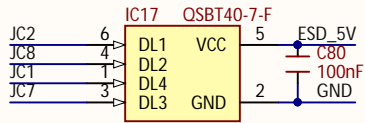
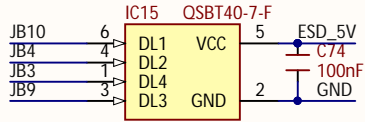
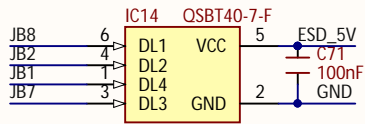
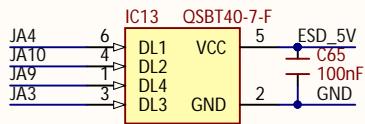
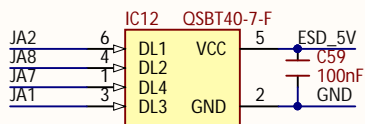




Title DSDB		Rev C Copyright 2016
Circuit MXP conn, Displays		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 2 out of 18		



Title DSDB		Rev C
Circuit ESD&OV Protection		Copyright 2016
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 3 out of 18		

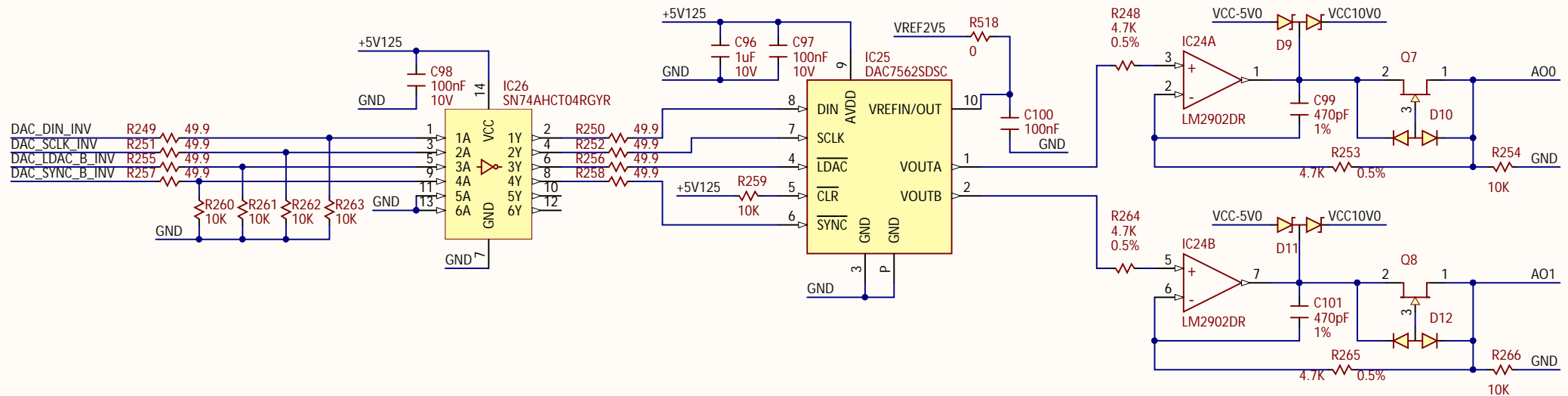


Title DSDB		Rev C Copyright 2016
Circuit ESD&OV Protection		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 4 out of 18		



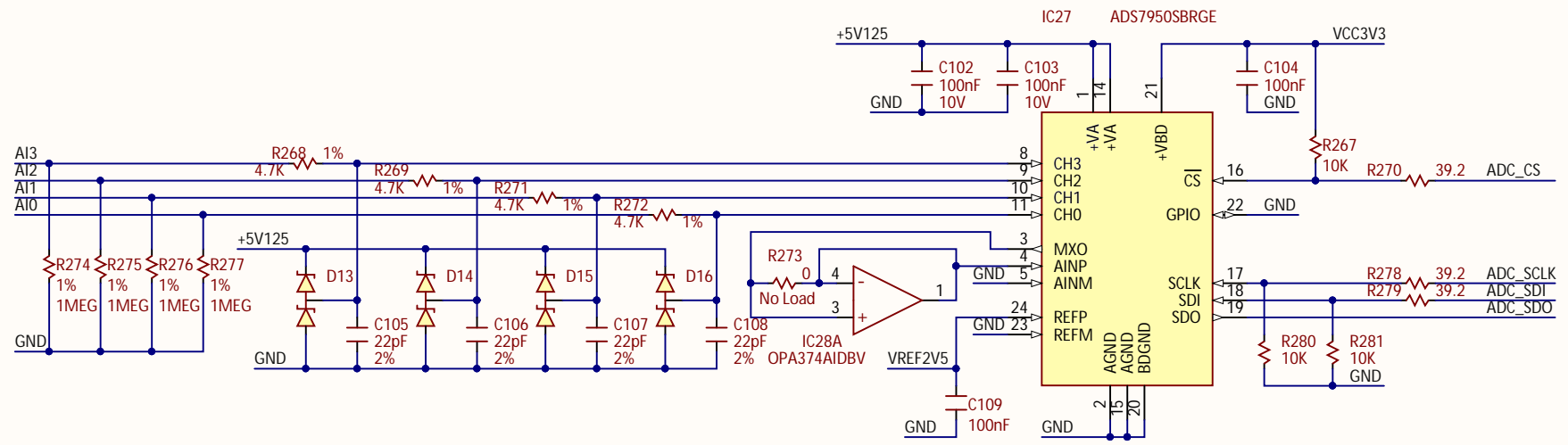
A

A



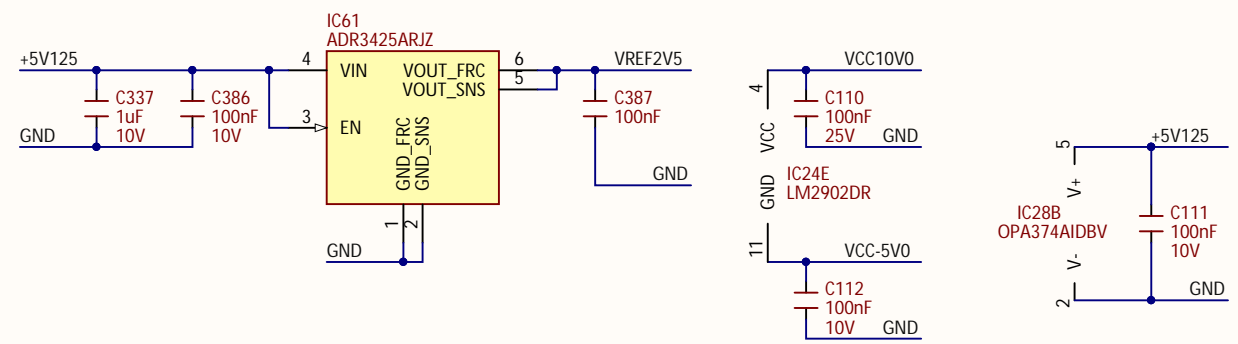
B

B



C

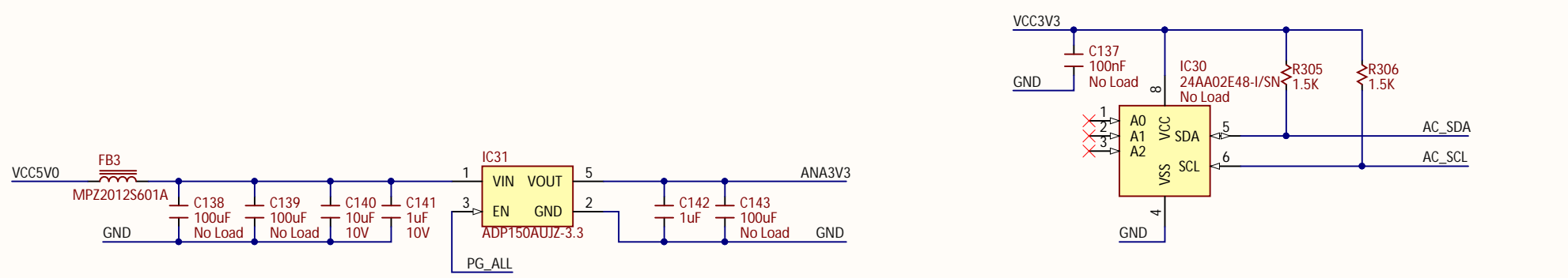
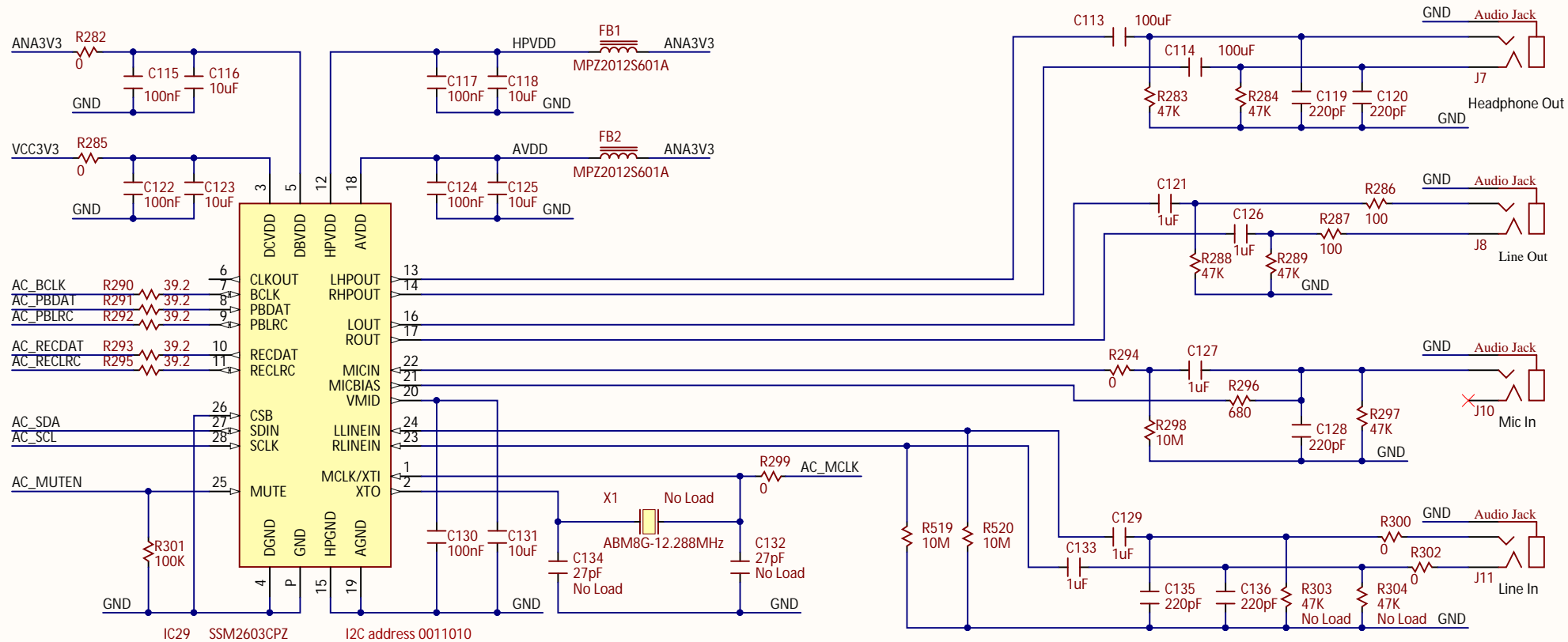
C



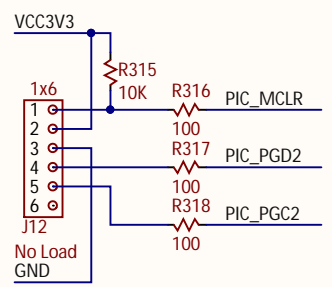
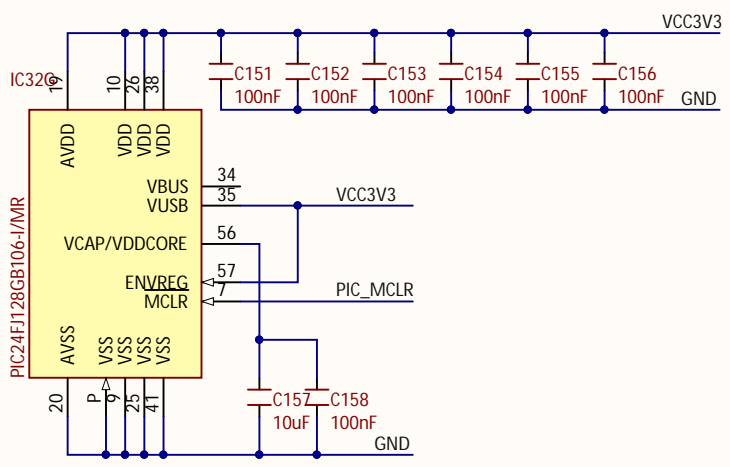
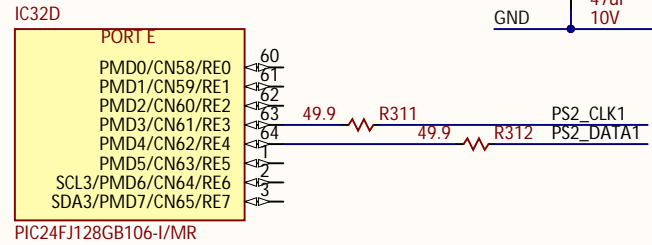
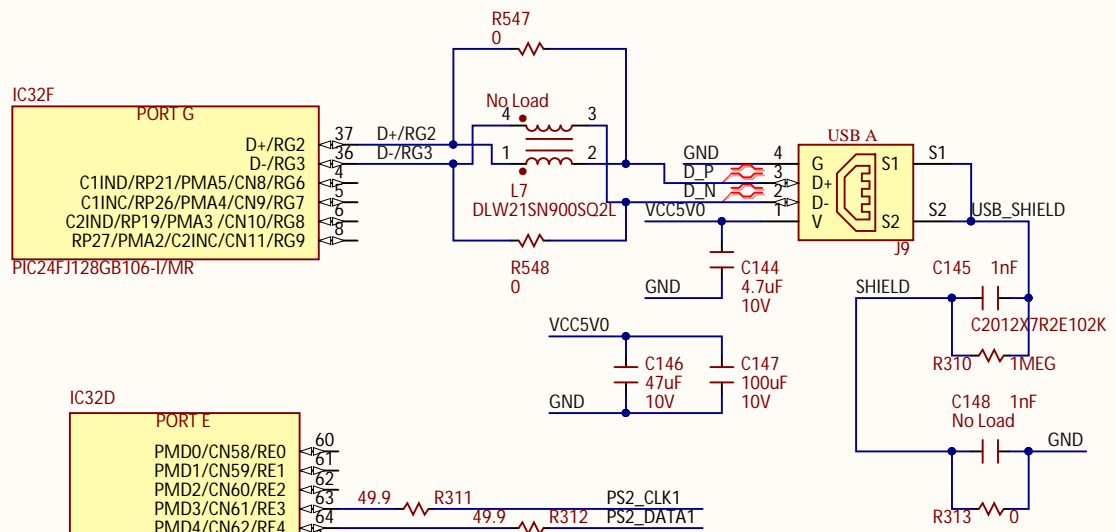
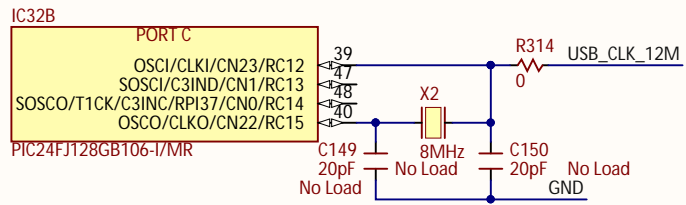
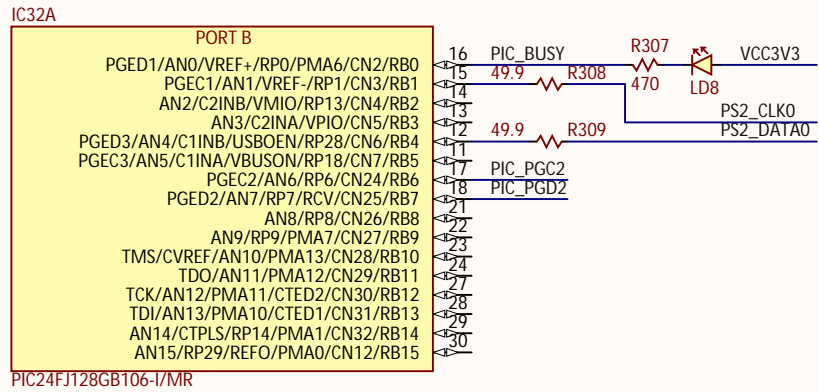
D

D

Title DSDB		Rev C
Circuit MXP Analog		Copyright 2016
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 6 out of 18		




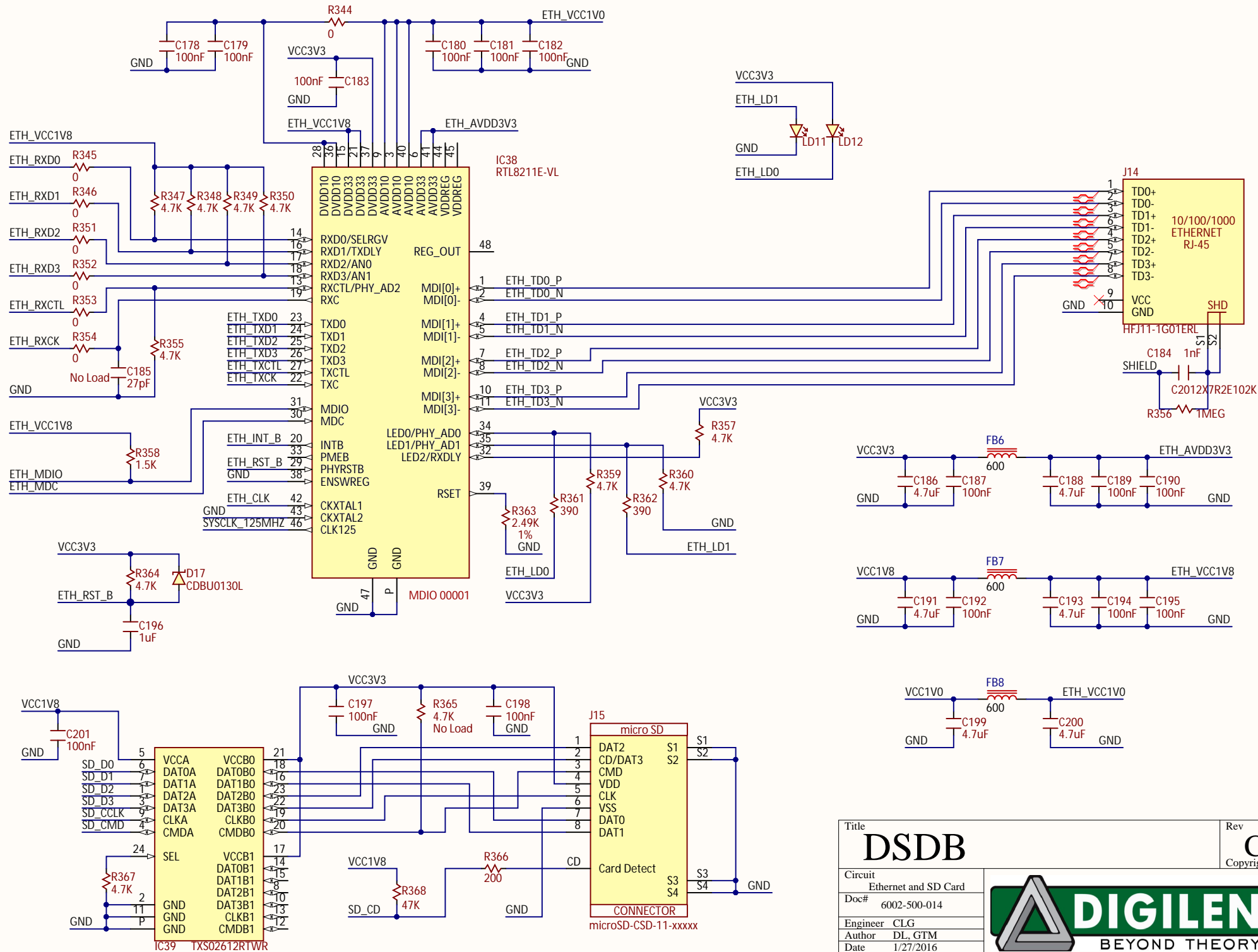
Title DSDB		Rev C
Circuit Audio Codec		Copyright 2016
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 7 out of 18		



Title DSDB		Rev C Copyright 2016
Circuit USB HID		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 8 out of 18		

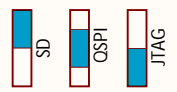
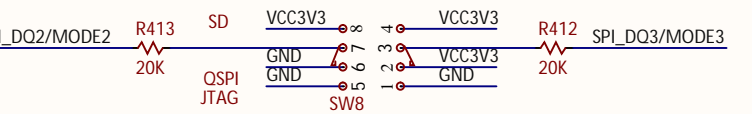
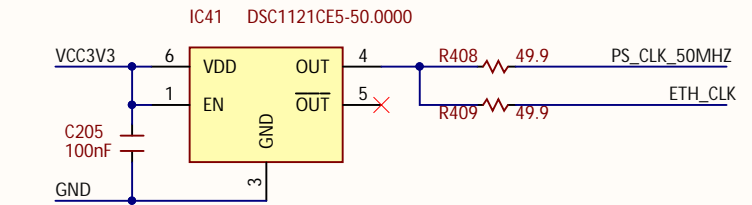
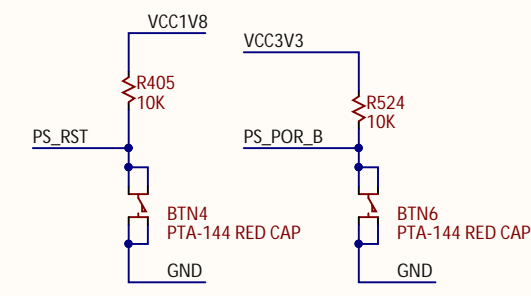
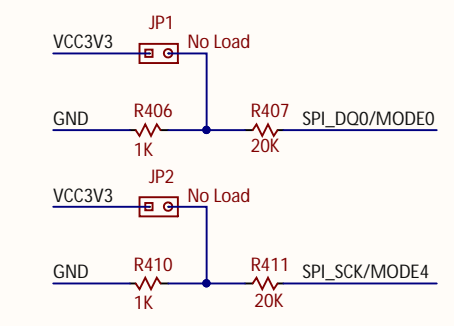
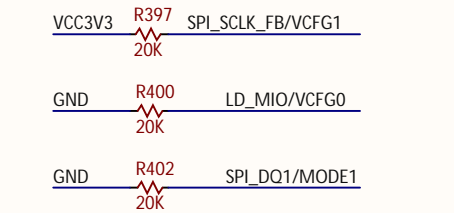
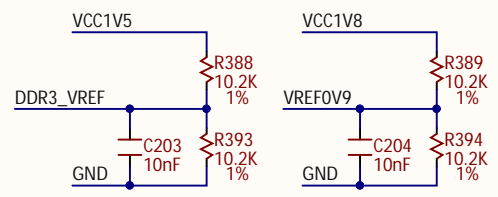
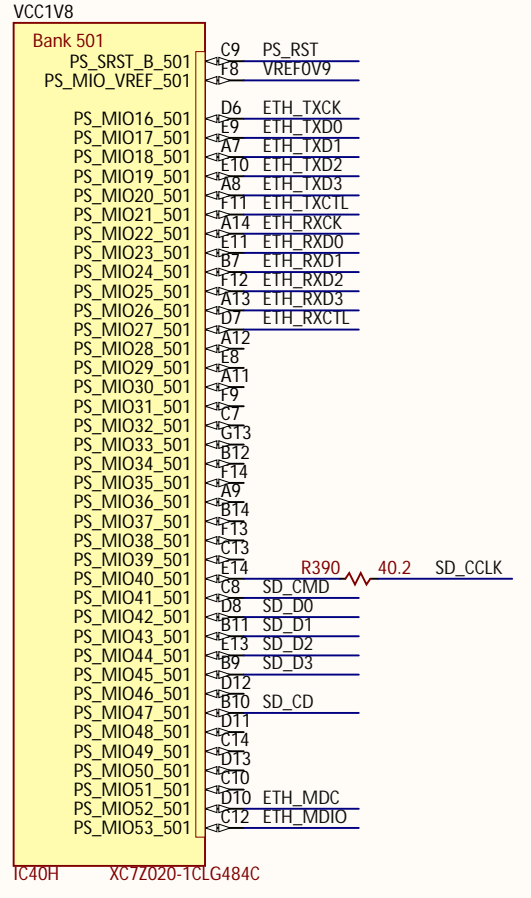
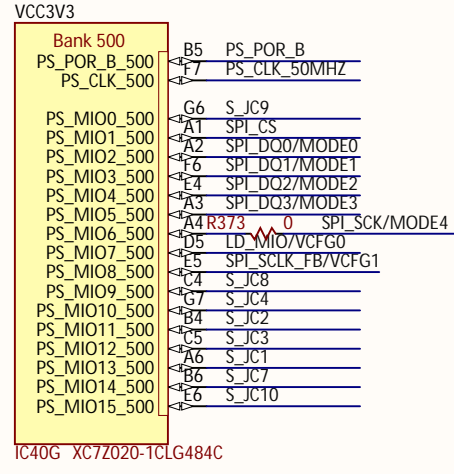
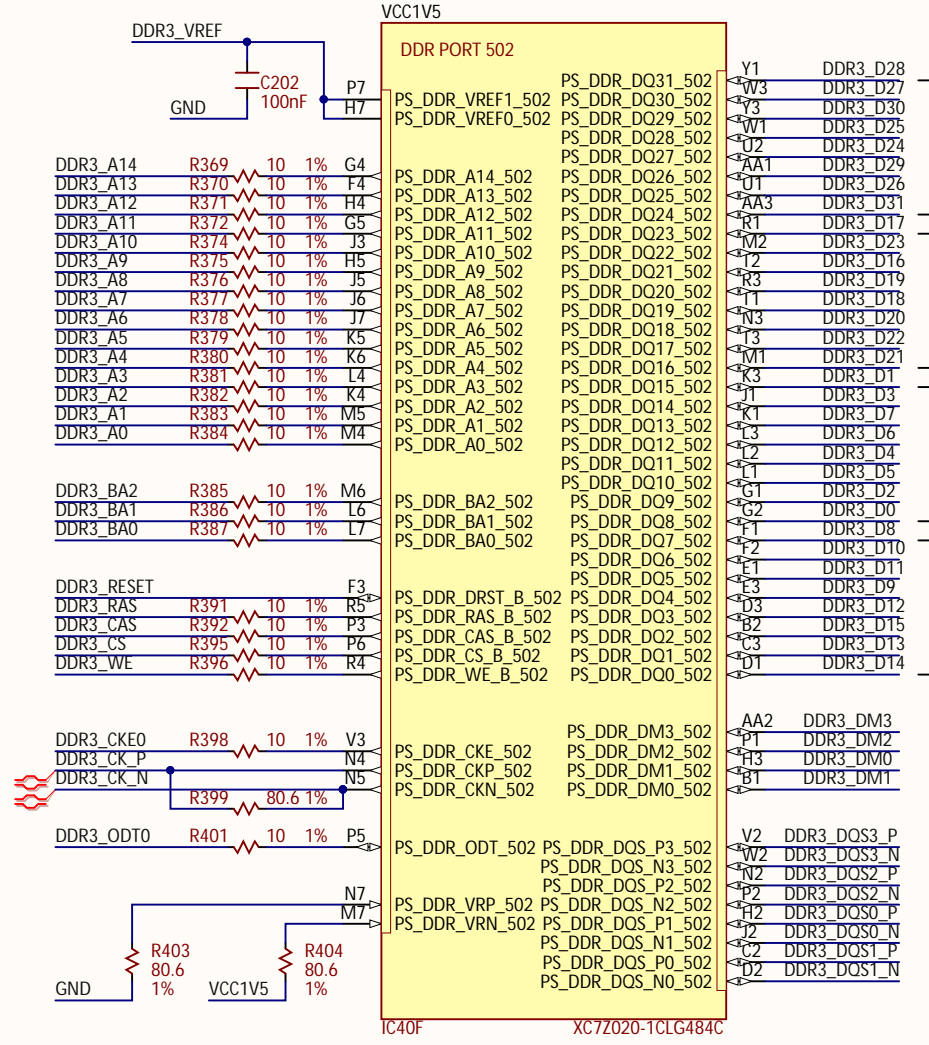
This Page Intentionally Left Blank

Title DSDB		Rev C Copyright 2016
Circuit USB PROG, UART		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 9 out of 18		

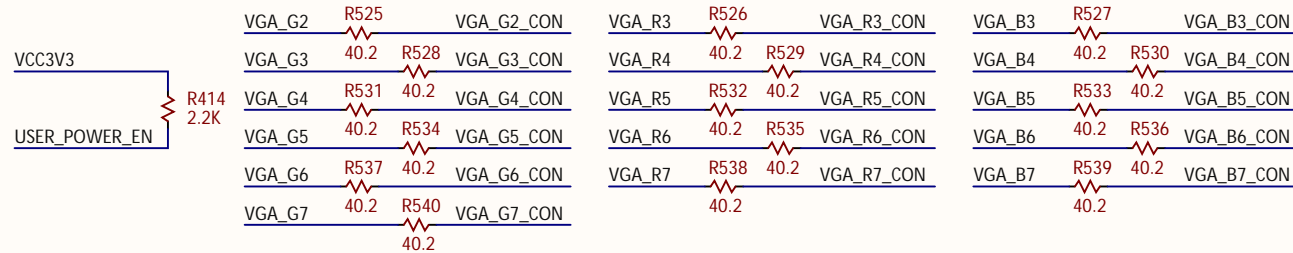
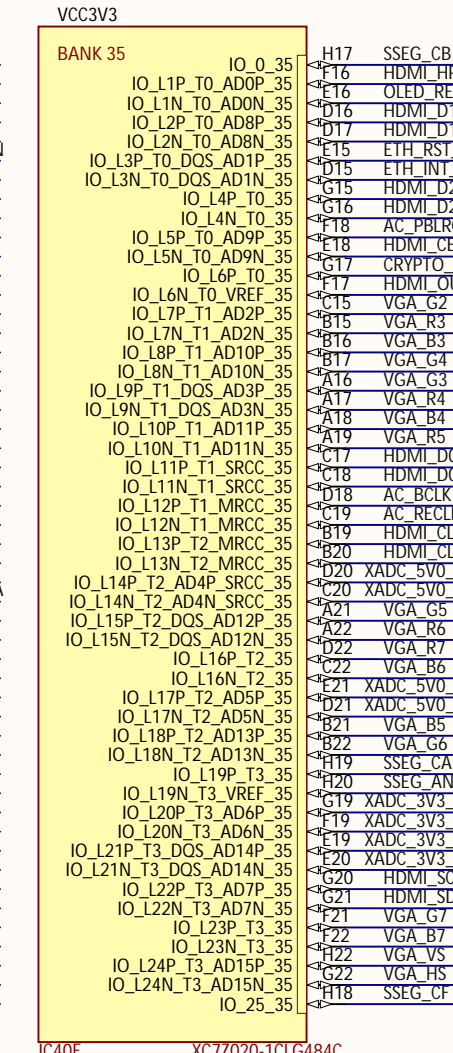
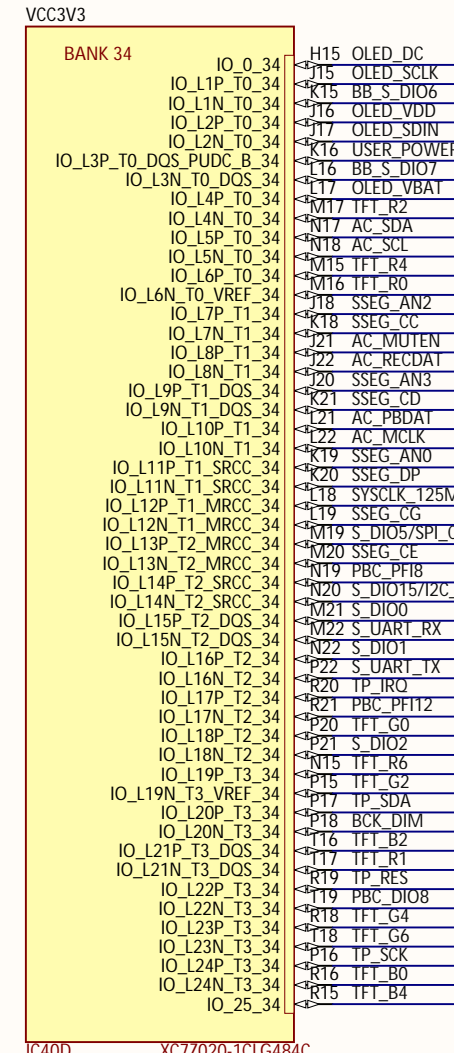
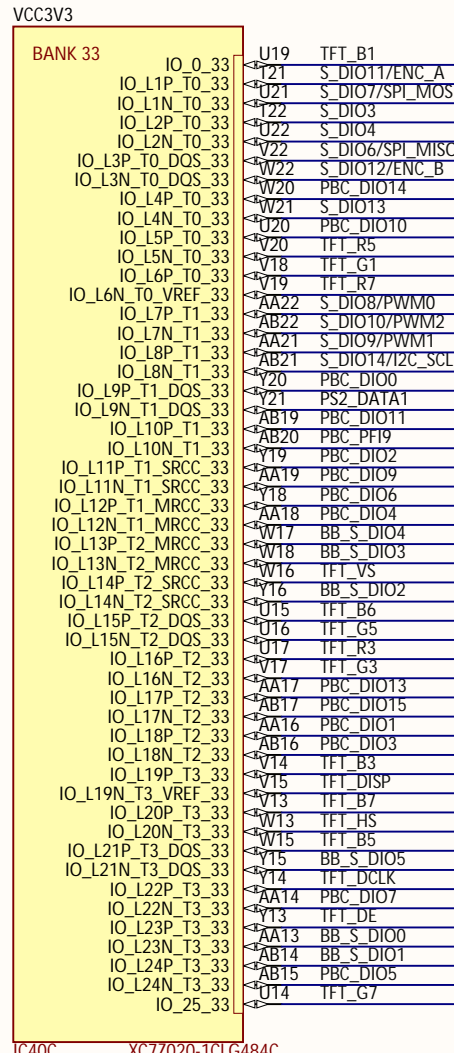
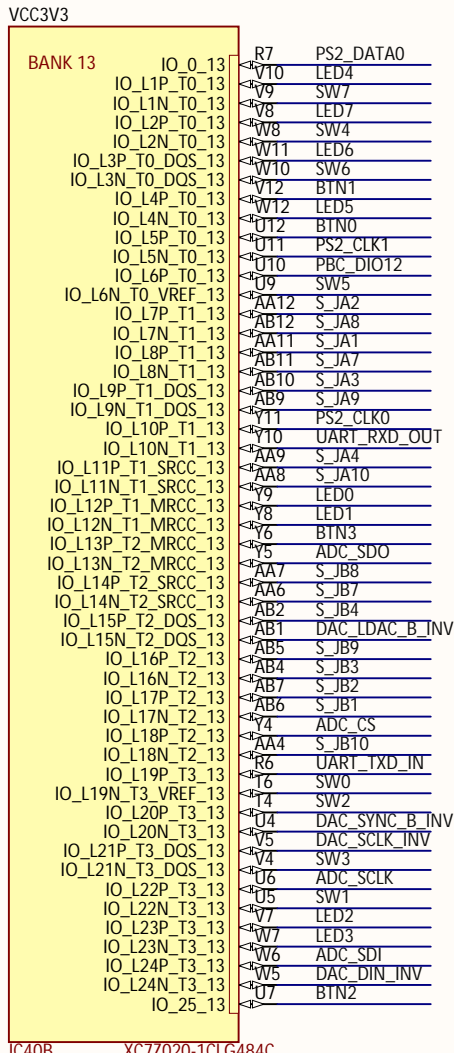


Title		Rev
DSDB		C
Circuit		Copyright 2016
Ethernet and SD Card		
Doc#	6002-500-014	
Engineer	CLG	
Author	DL, GTM	
Date	1/27/2016	
Sheet#	10 out of 18	




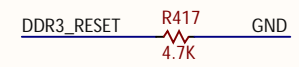
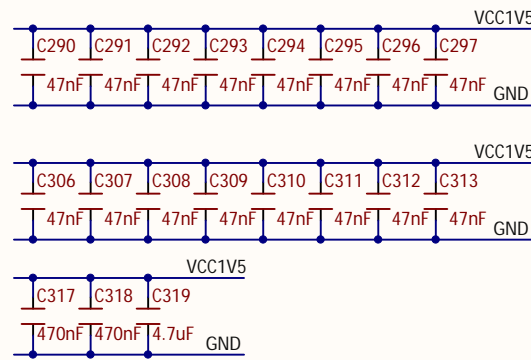
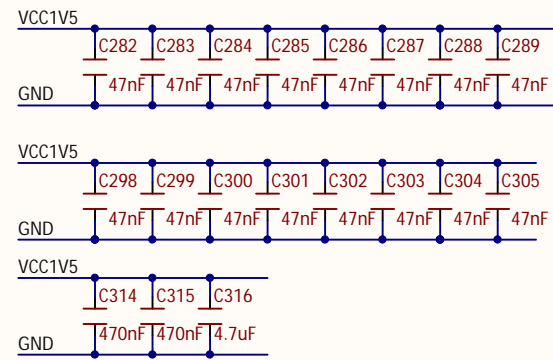
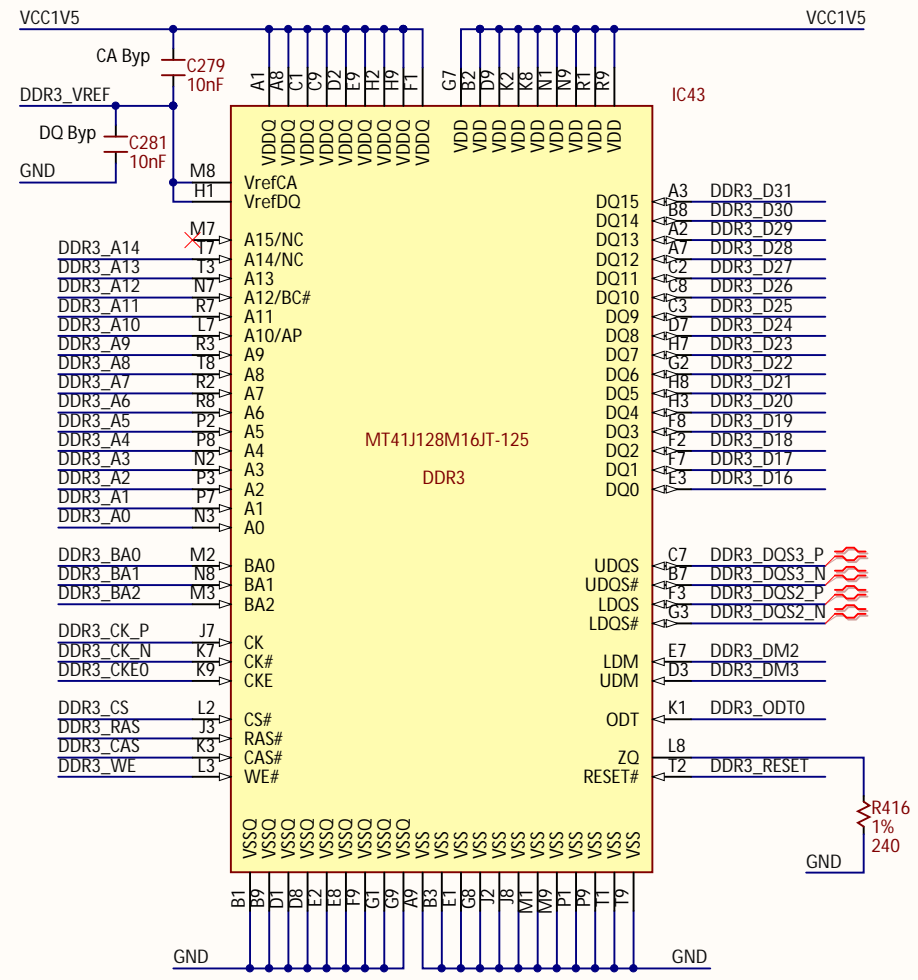
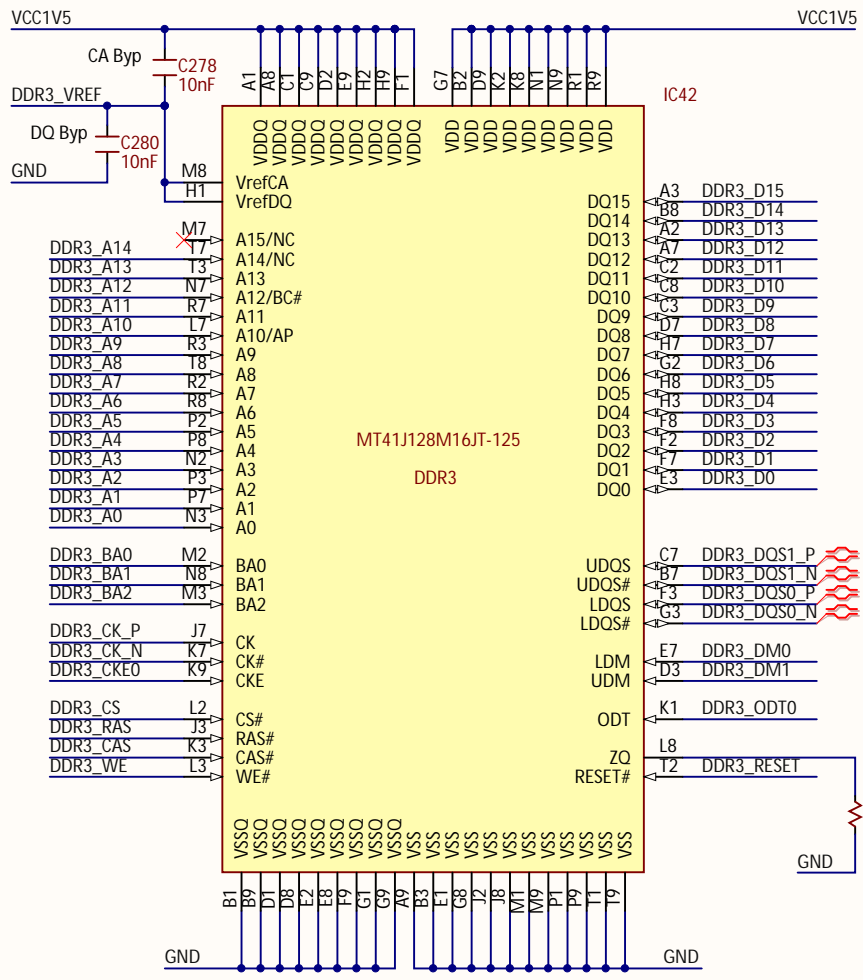


Title DSDB		Rev C
Copyright 2016		
Circuit DDR and MIO Banks	Doc# 6002-500-014	
Engineer CLG	Author DL, GTM	
Date 1/27/2016	Sheet# 11 out of 18	

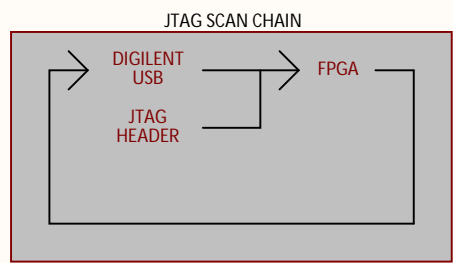
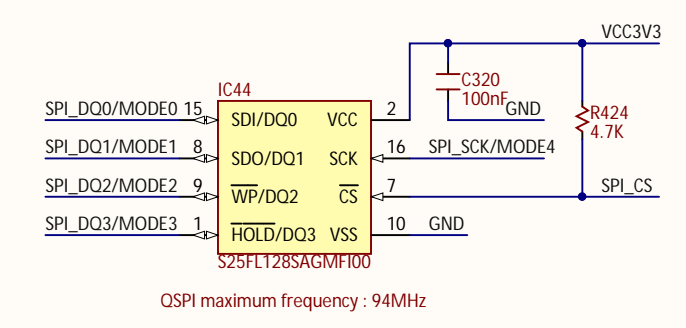
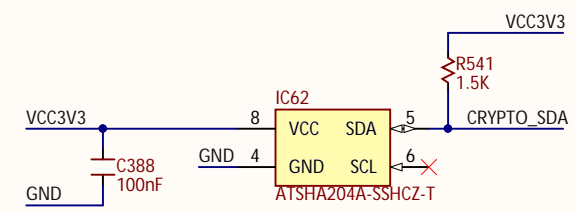
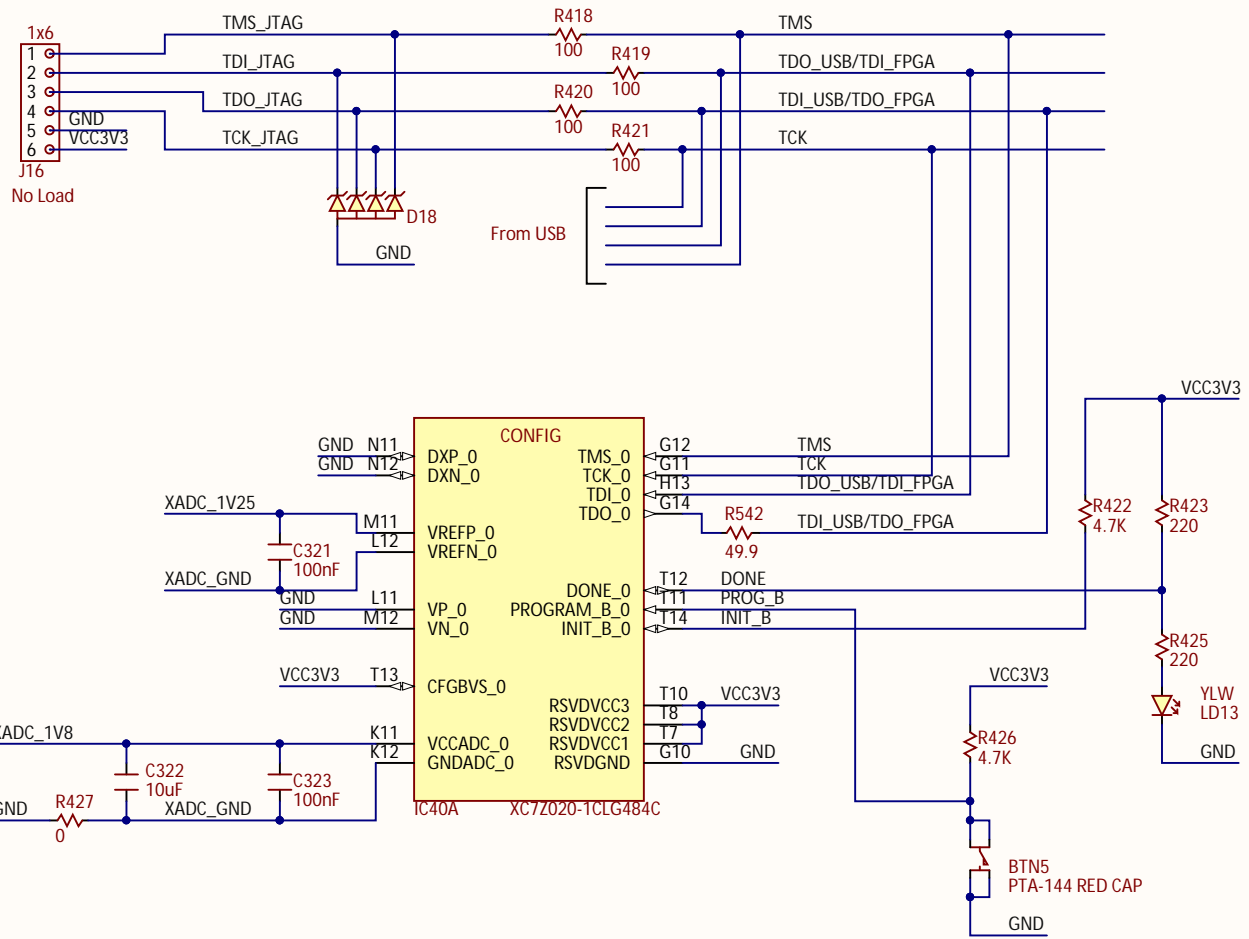


Title		Rev	
DSDB		C	
Circuit		Copyright 2016	
FPGA Banks			
Doc#		6002-500-014	
Engineer		CLG	
Author		DL. GTM	
Date		1/27/2016	
Sheet#		12 out of 18	



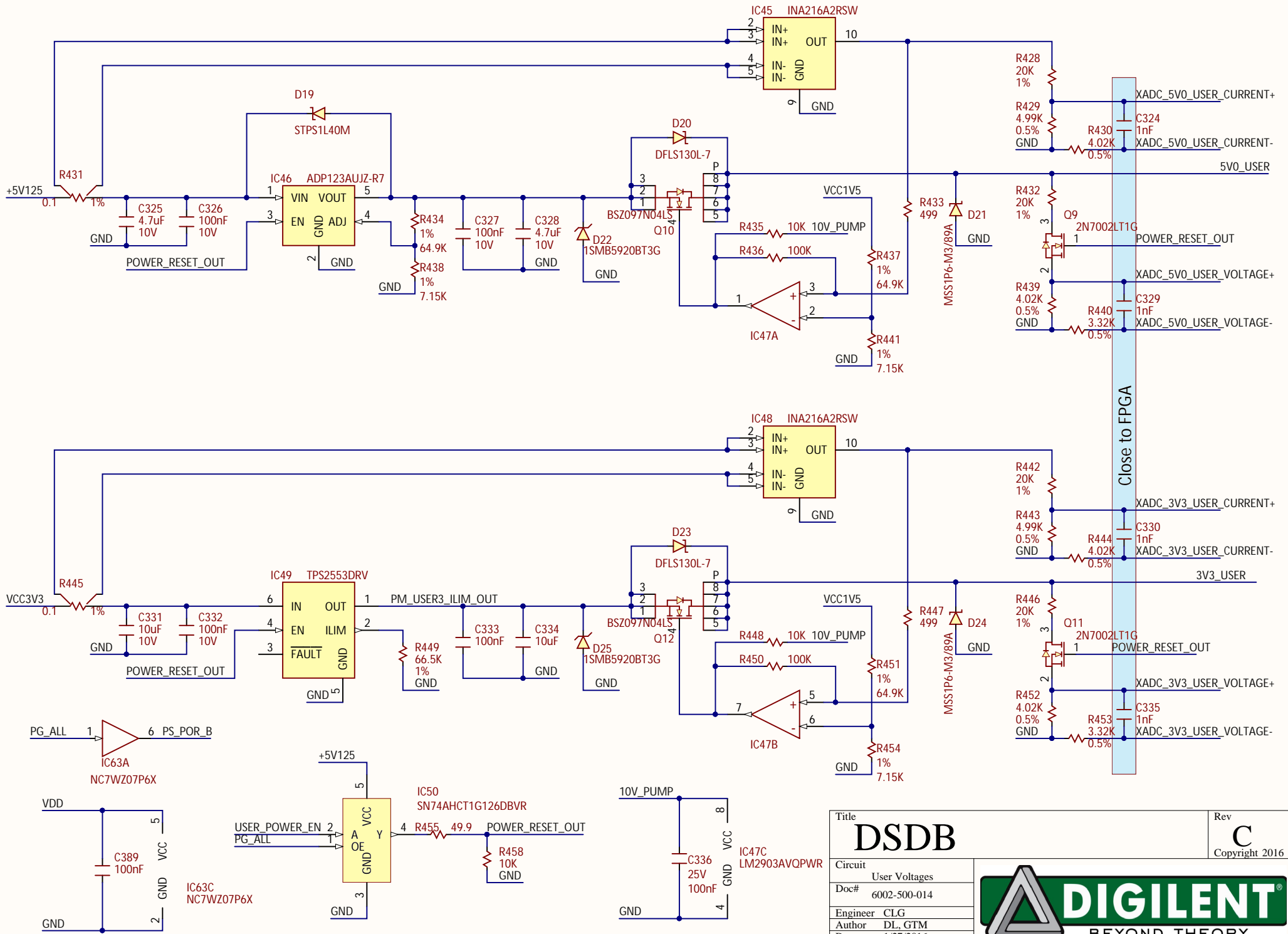


Title DSDB		Rev C Copyright 2016
Circuit DDR3 Memory		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 14 out of 18		




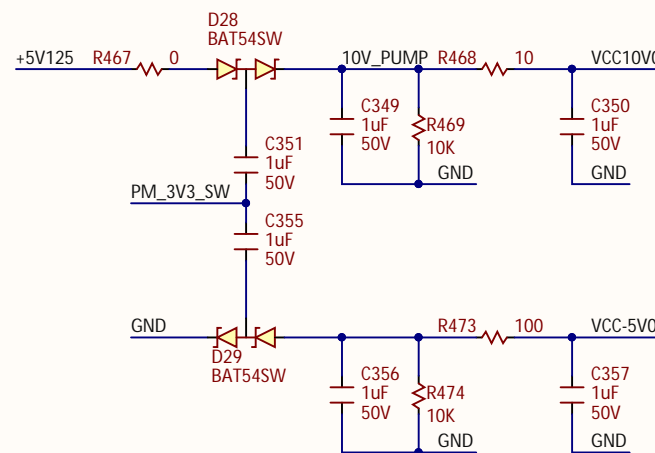
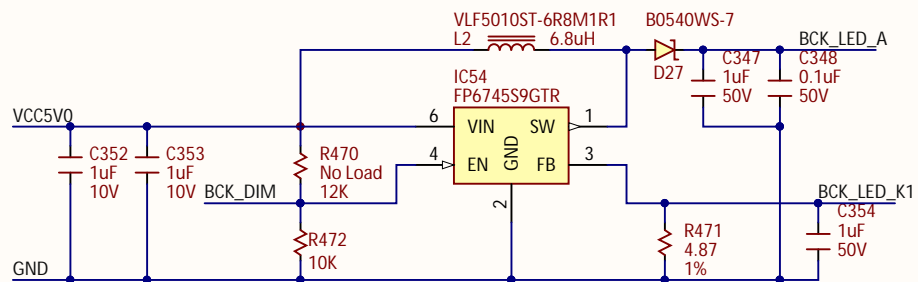
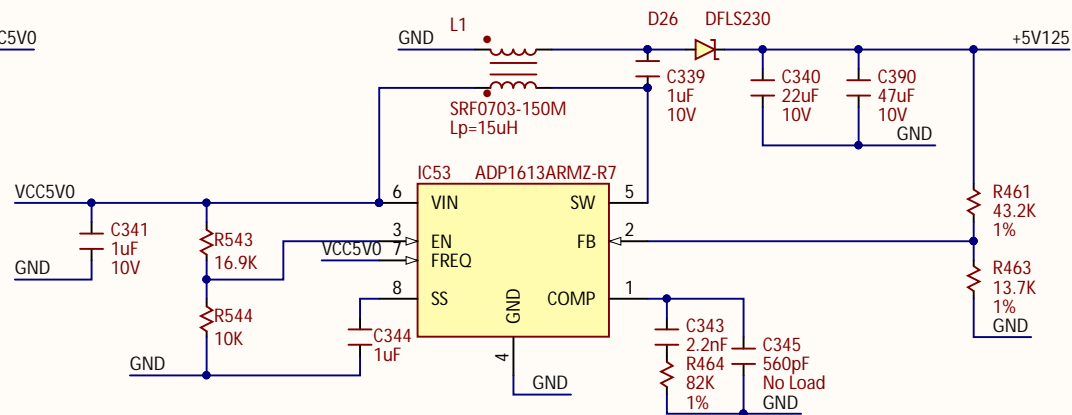
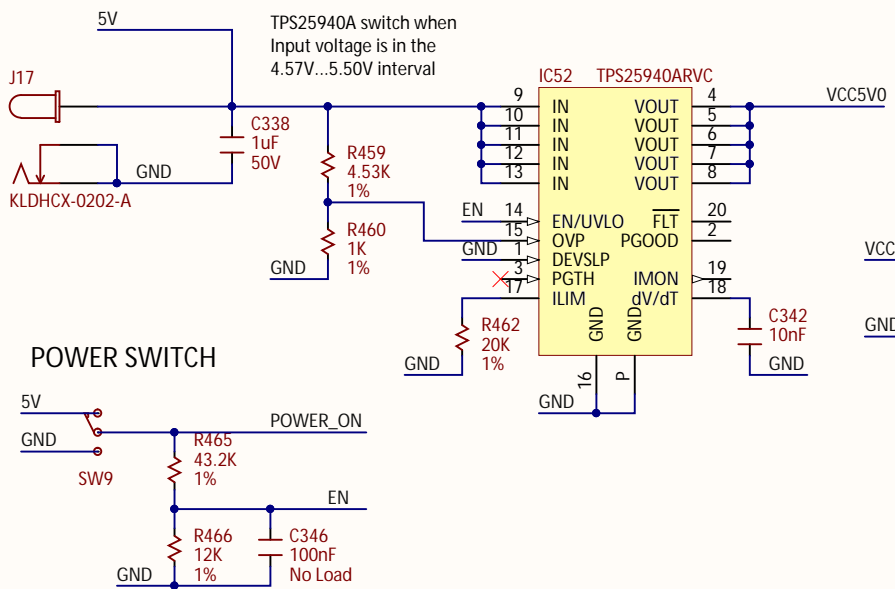
Title DSDB		Rev C Copyright 2016
Circuit FPGA Configuration, Flash		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 15 out of 18		




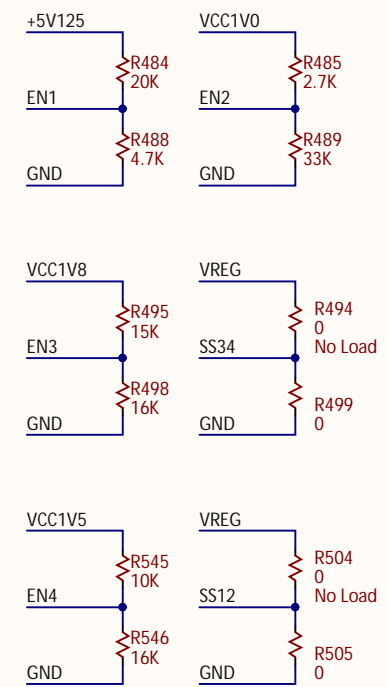
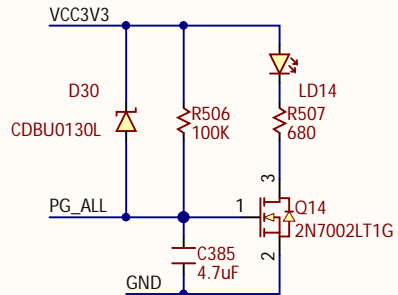
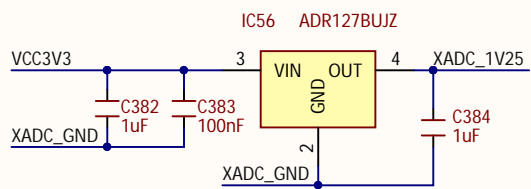
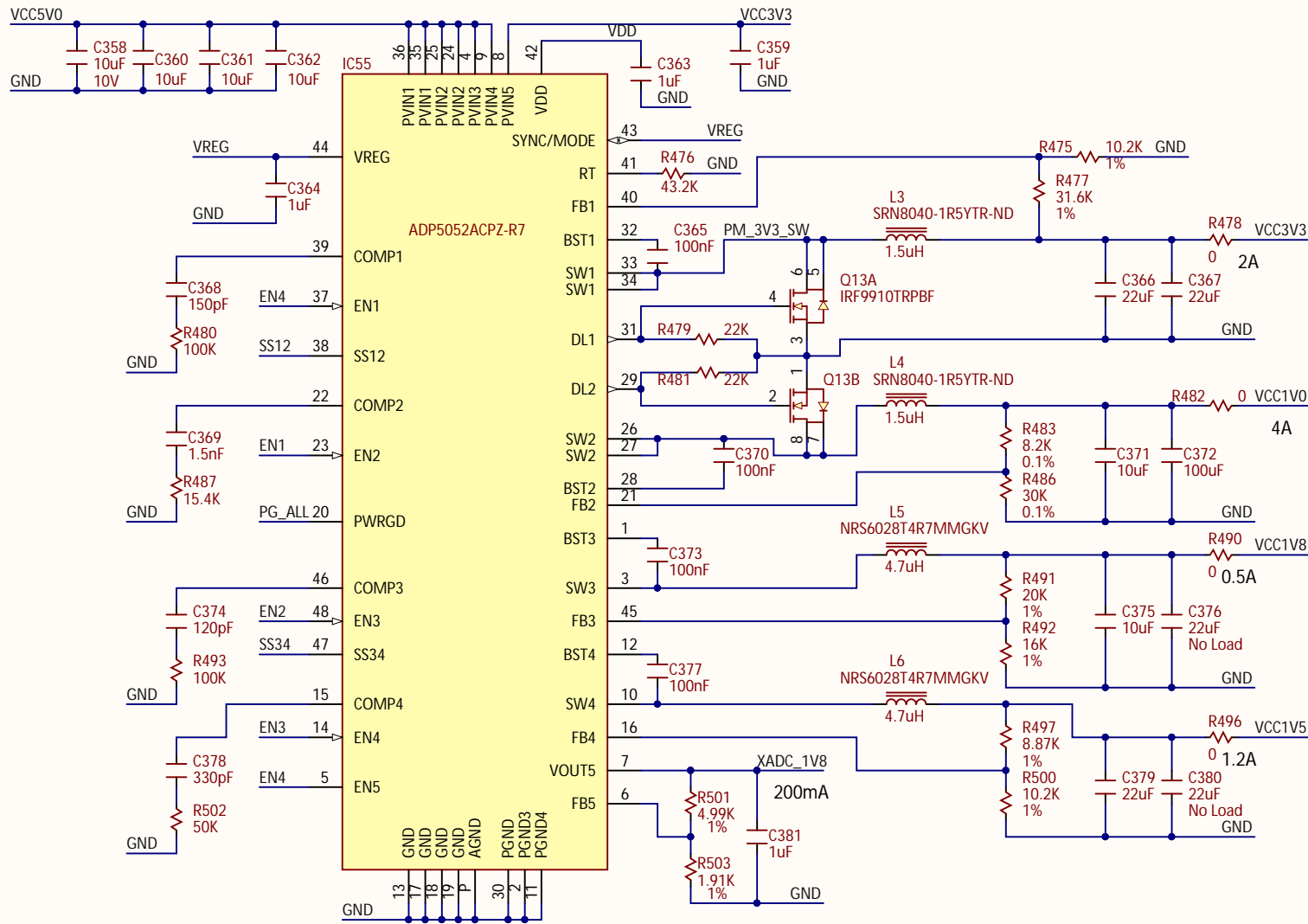


Title DSDB		Rev C
Doc# 6002-500-014		Copyright 2016
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 16 out of 18		


DIGILENT
 BEYOND THEORY



Title DSDB		Rev C Copyright 2016
Circuit Power Regulation		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 17 out of 18		



Title DSDB		Rev C Copyright 2016
Circuit Power Regulation		
Doc# 6002-500-014		
Engineer CLG		
Author DL, GTM		
Date 1/27/2016		
Sheet# 18 out of 18		